Geometry scaling improvement of ASM-HEMT model for GaN

Lucas PRAT, Fadi Zaki – AKB 2023

Last year presentations on GaN

- G. U’Ren: "Heterogeneous GaN on RFSOI“
- F. Zaki, L. Iogna-Prat, H. Saleh and G. U'Ren: "GaN ASM-HEMT DC Geometry Scaling Development"

Both presentations are available here:
https://www.iee.et.tu-dresden.de/iee/eb/forsch/AK-Bipo/ak_bipo_bei.html

Outline

1 Context and motivation

2 ASM-HEMT: model overview and previous results

3 New test chip using a different GaN technology

4 Results on reference DUT (fixed geometry): *DC linear/saturation conditions; Capacitances; S-parameters;*

5 Width Scaling improvement: *scaling rules development and final results (DC)*

6 On-going work: *current model weaknesses; width Scaling development for the capacitances*

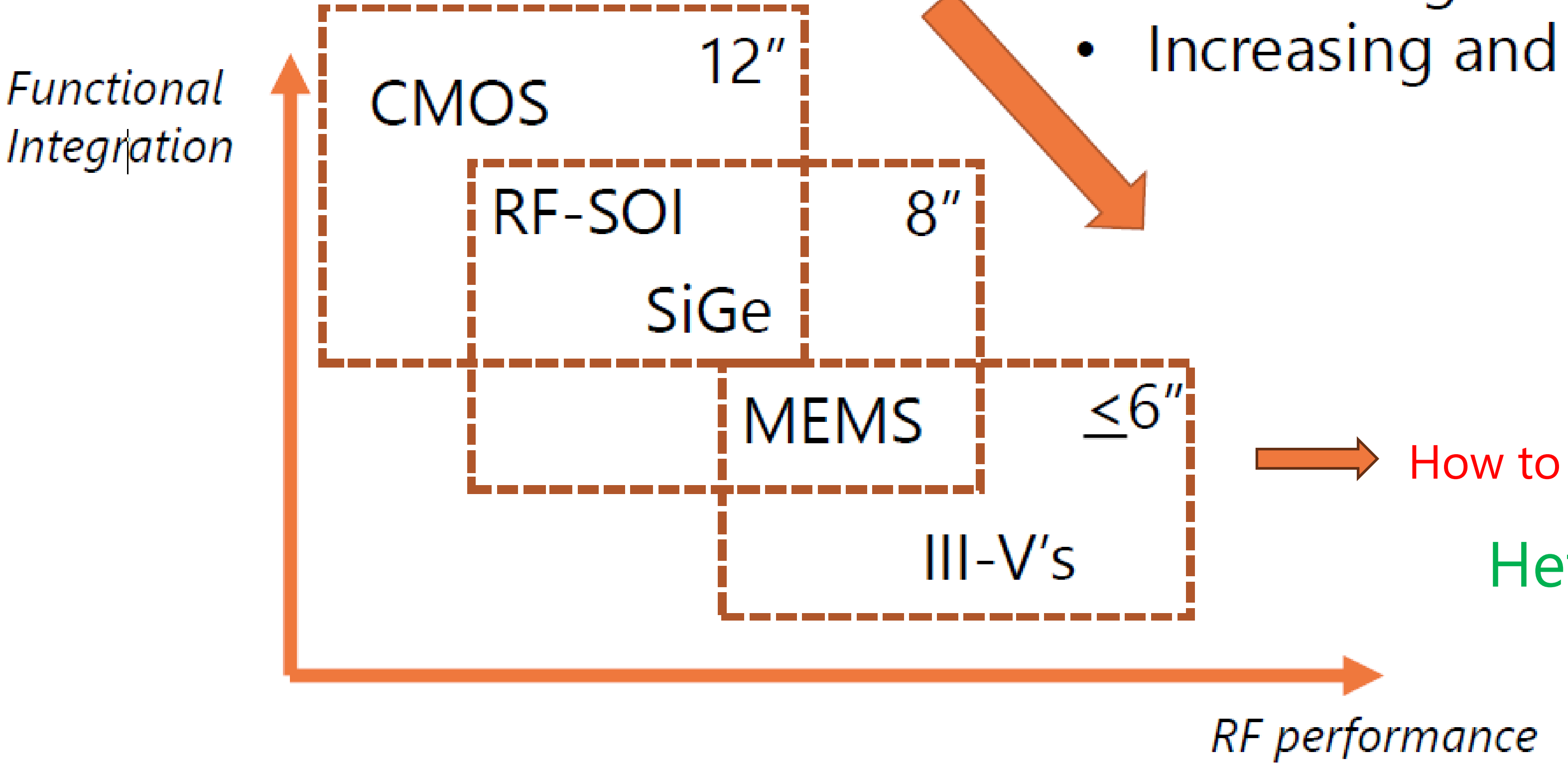
7 Conclusions and next steps

Context and motivation

Why GaN?

XFAB does not have any RF GaN technology in its portfolio, but…

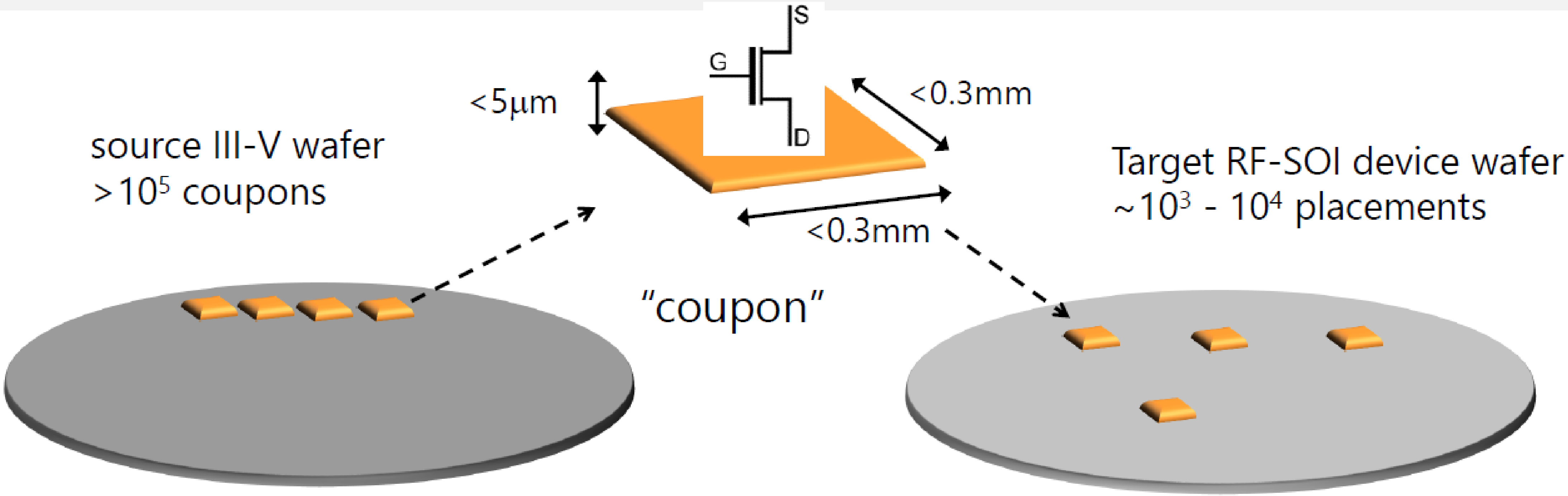
- Decreasing functional integration
- Increasing and compelling RF figures of merit



How to overcome the low integration?

Heterogeneous GaN on RFSOI

Wafer level integration of III-V's



- Efficient area utilization of a high value source material
- Coupon contains 1 or more components

G. U'Ren, RFIC workshop 2022

RF-GaN – a wafer level heterogeneous integration approach

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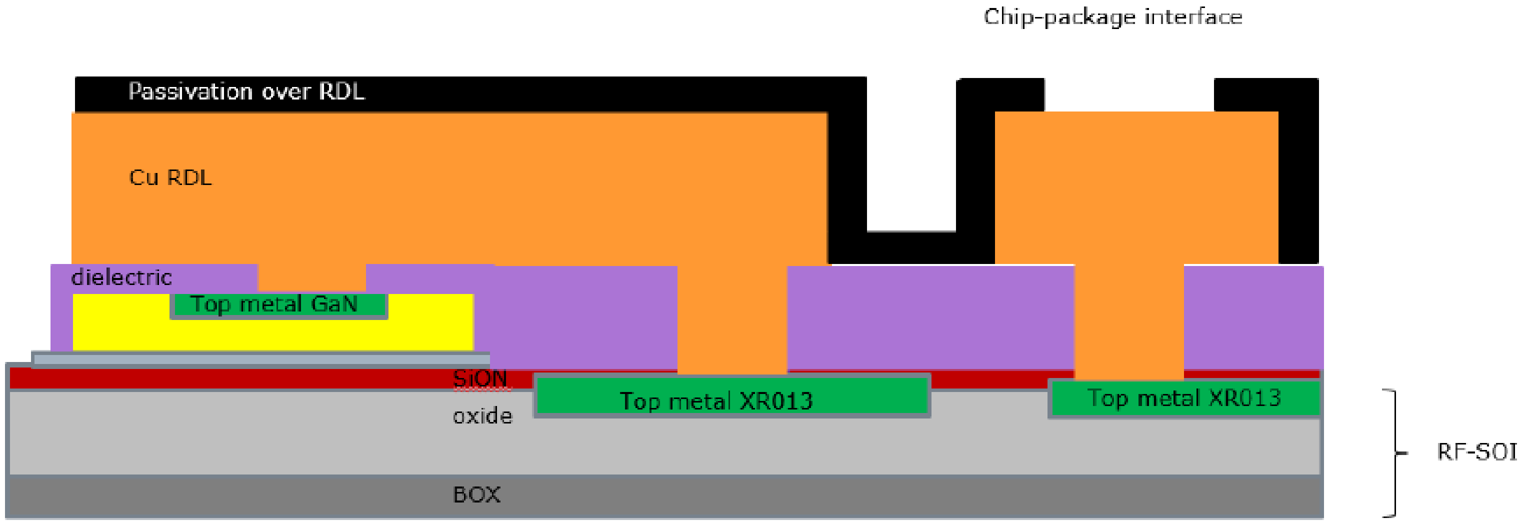


Cartoon of the co-integration method in cross-section (not to scale)

- GaN coupon placed face-up
- Cu RDL connects GaN to RF-SOI.
- RDL / RF-SOI serves as the chip-package interface
- Interconnect density on the order of micrometers

F. Drillet *et al.*, "RF SPST Switch Based on Innovative Heterogeneous GaN/SOI Integration Technique," *2020 15th European Microwave Integrated Circuits Conference (EuMIC)*, 2021, pp. 117-120.

J. Loraine, H. Saleh, F. Drillet, O. Sow, I. Lahbib and G. U'Ren, *"5.9-7.1GHz High-Linearity LNA Using Innovative 3D Device Level Co-Integration of GaN HEMT and RF-SOI," 2021 IEEE MTT-S International Microwave Symposium (IMS), 2021, pp. 20-22, doi: 10.1109/IMS19712.2021.9574971.*

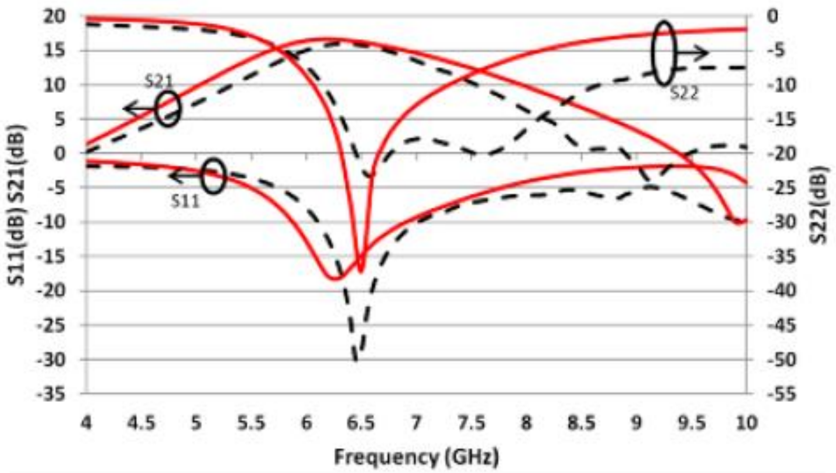
LNA results: small signal

- C4/bump and Flip chip mounting on PCB
- De-embedding through line on top

PCB

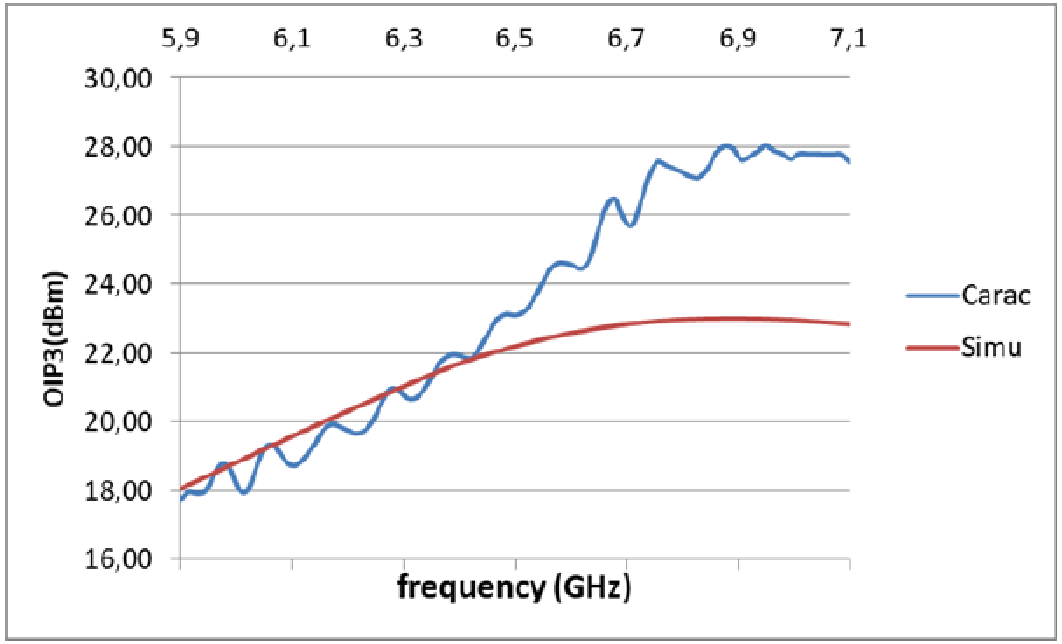
Die

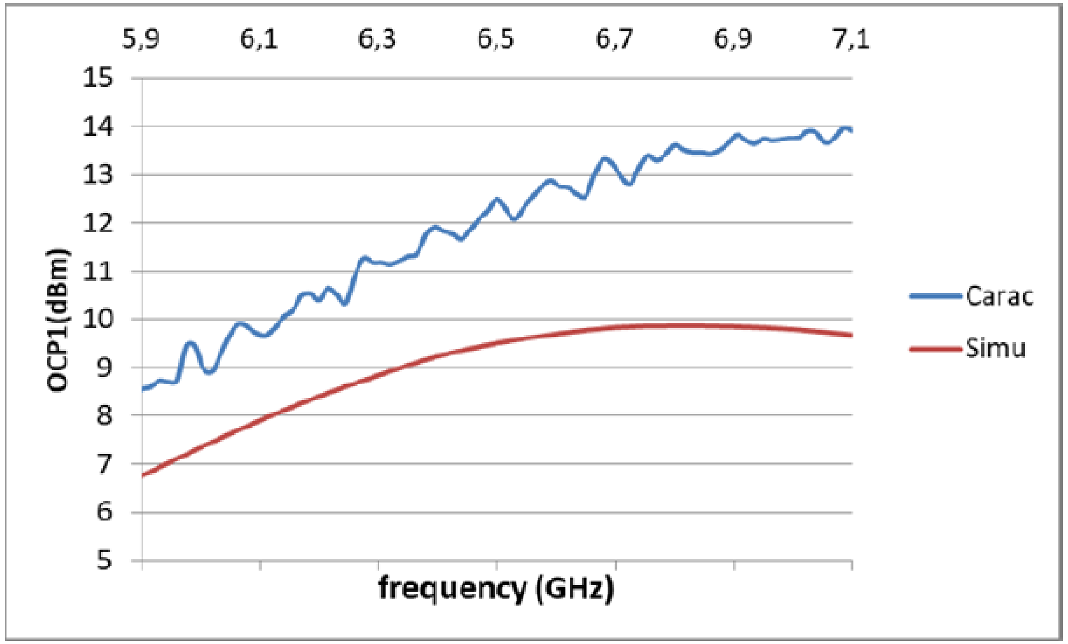
S-parameter results



	Measurement	Simulation
Frequency (GHz)	5.9 – 7.1 (band n96)	
S11 (dB)	-6.6 / -9.3	-10.5 / -8.6
S22 (dB)	-6/-19.9	-6.9 / -11.8
S21 (dB)	15.7*	16.2*
DC consumption (mW)	72.6	

LNA results: linearity





- Bias conditions: Id = 12.5mA with Vcas = 1.2V
- Simulations done using the available GaN HEMT model (external PDK)

- Many GaN foundries are not yet using standard CMC compact models -> opportunity for improvement with ASM-HEMT

ASM-HEMT

model overview

CMC GaN model

Available models:

	Empirical	Physics-based (new)	ANN-based
Models	Angelov-GaN, EEHEMT	ASM-HEMT MVSG	DynaFET
CMC Standard		✓	
Scalable, W/L/NF	✓ *	✓	✓ *
Does not require process info	✓	*	✓
Simple extraction flow	✓		
Good DC/S-par fit	✓	✓	✓
Large signal across different bias		✓	✓
Simulation robustness		✓	✓

Table from Keysight presentation comparing the existing model for GaN.
Slides presented on 2021.04.08

ASM-HEMT model overview

ASM-HEMT model composition:

Core channel charge model → Core terminal current model → Models for real device effects

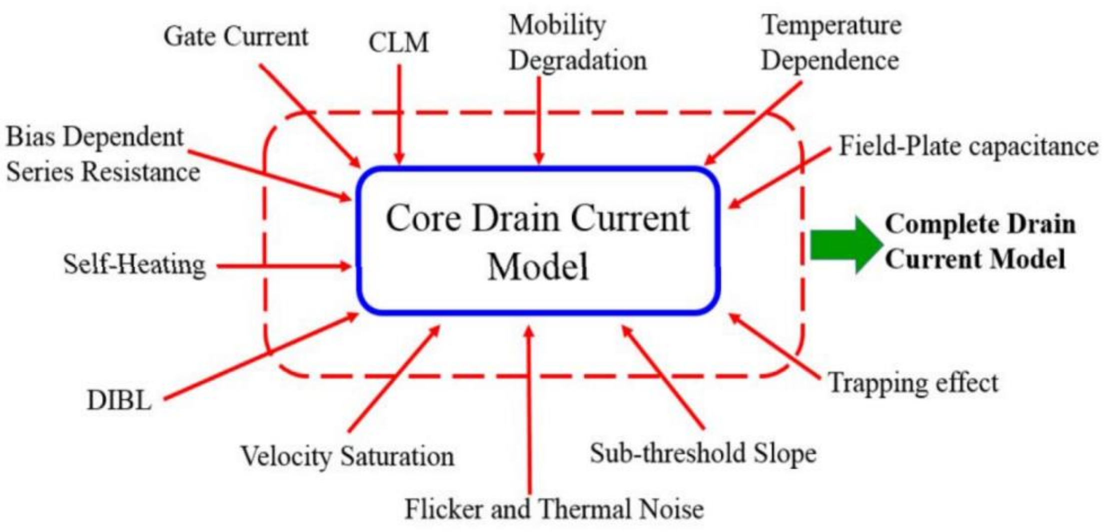


Figure from 32nd AK-Bipolar Workshop, slides presented on Nov. 14/15, 2019

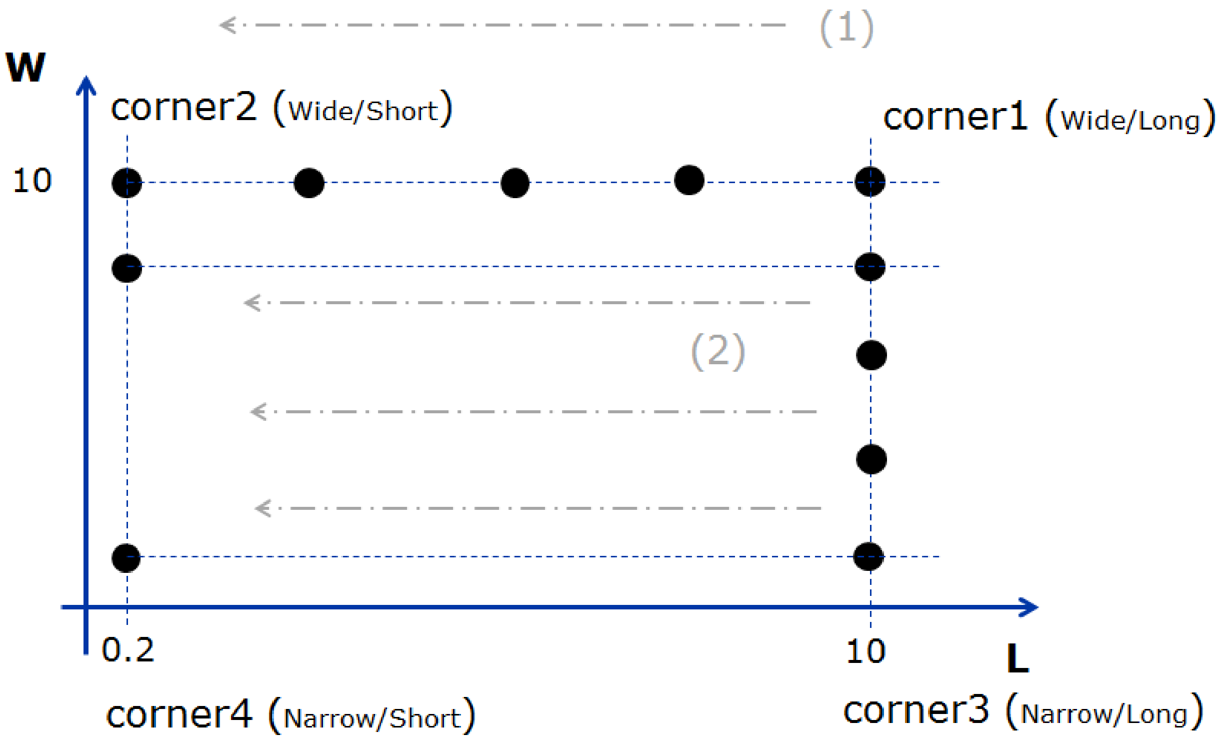
Model features:

- *Gate current.*
- *Mobility field dependence.*
- *Drain-induced barrier lowering.*
- *Subthreshold-slope degradation.*
- *Non-linear series resistance.*
- *Channel-length modulation.*
- *Velocity saturation effect.*
- *Self-heating effect.*
- *Temperature dependence.*
- *Trapping (by RC network sub-circuits).*
- *Flicker and thermal noise.*

ASM-HEMT model overview

- The model seems to be good … is there something missing ?

Yes, an accurate scaling modeling



At the industrial level, geometrical scaling is a highly significant step in modeling:

It is crucial for the model to accurately predict the behavior of the device when subjected to **length** **and** **width** **scaling**.

ASM-HEMT Geometry Scaling Development

W scaling results:

Before DC Geometry Scaling implementation

By scaling rules implementation

<u>Example</u>:

$$\mu_{\text{eff}} = \frac{\mathbf{U_{0s}}(T)}{1 + \mathbf{UAs}.E_{y,eff} + \mathbf{UBs}.E_{y,eff}^{2}}$$

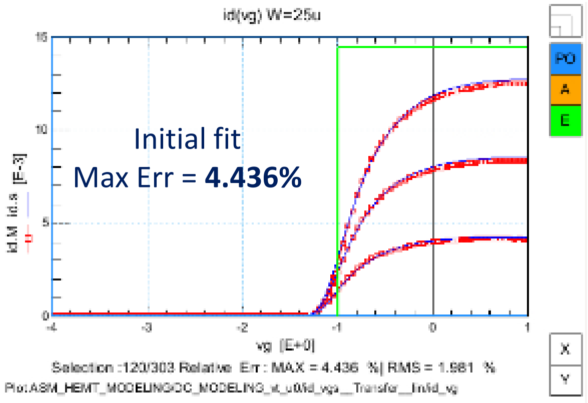
- U_{0s} Scaling rule example:

$$\mathrm{U_{0s}} = \mathrm{U_0}(T).\left[\frac{\mathrm{W_{EN}}}{\mathrm{W_E}}\right]^{\mathrm{U0VALEXP}}$$

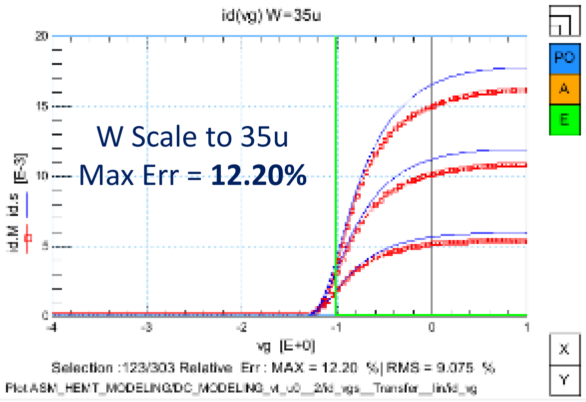
After DC Geometry Scaling implementation

Sim Vs measurements for DC characterisitics- before scaling

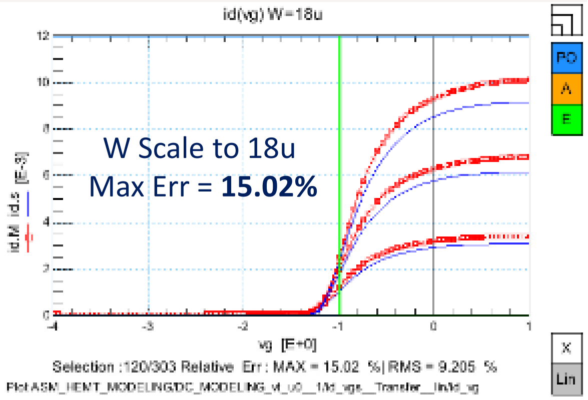
Initial fit for L100 **W25** NF2



W Scale for L100 **W35** NF2

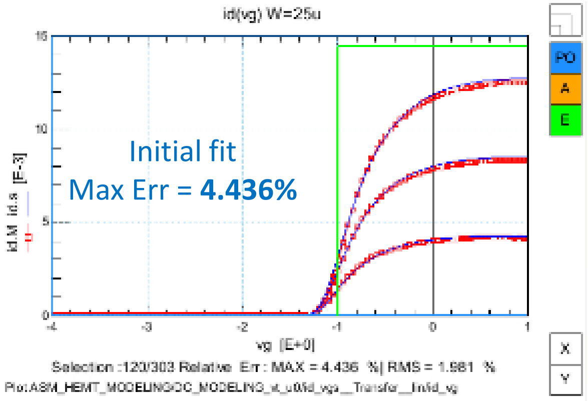


W Scale for L100 **W18** NF2

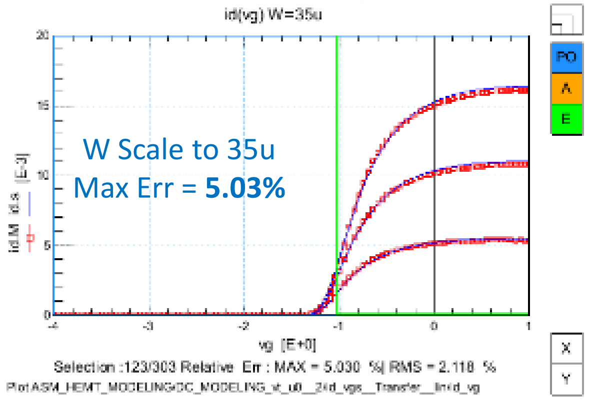


Sim Vs measurements for DC characterisitics- after scaling

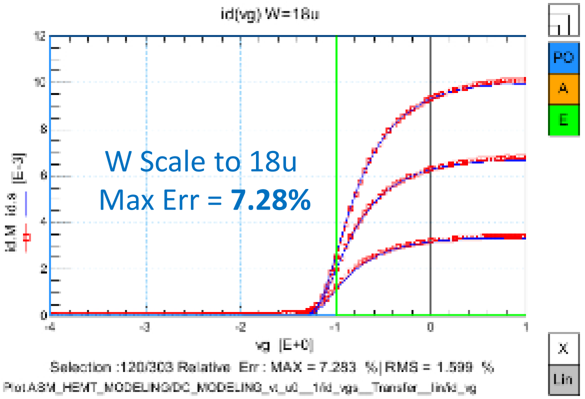
Initial fit for L100 **W25** NF2



W Scale for L100 **W35** NF2



W Scale for L100 **W18** NF2

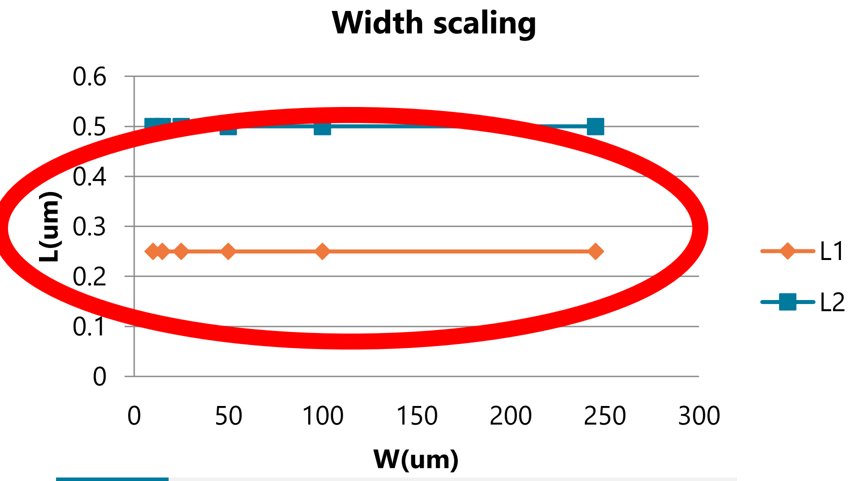


New test chip

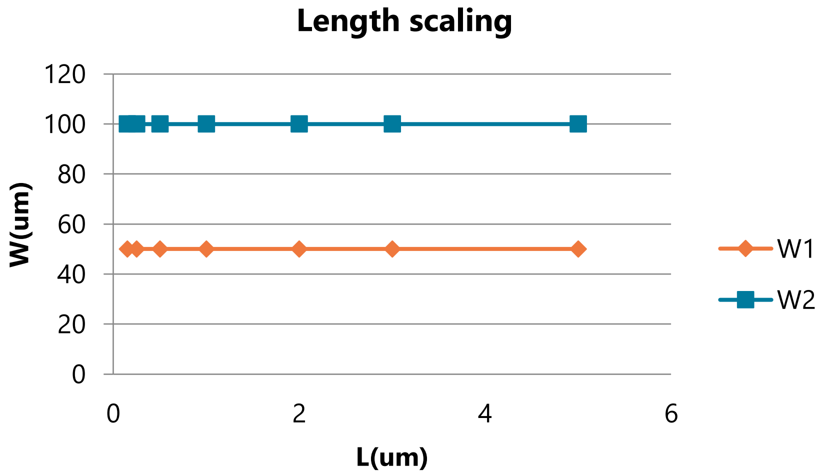
(different GaN technology, different foundry)

New test chip (different GaN tech, different foundry)

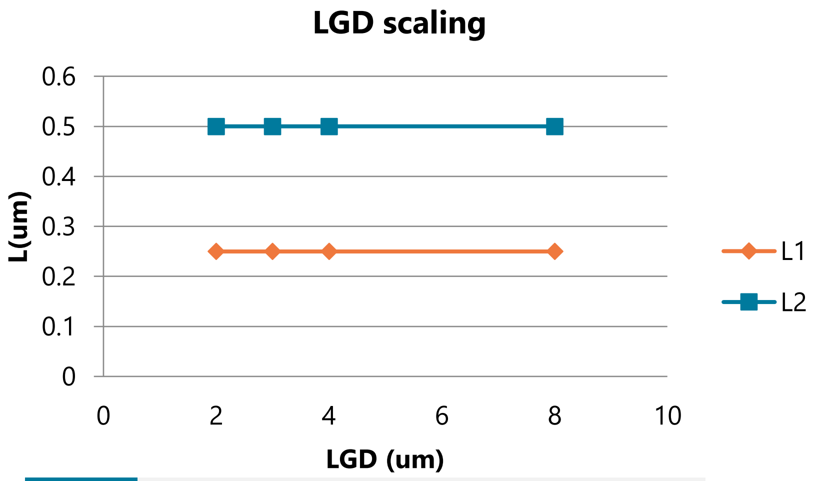
1 Width scaling



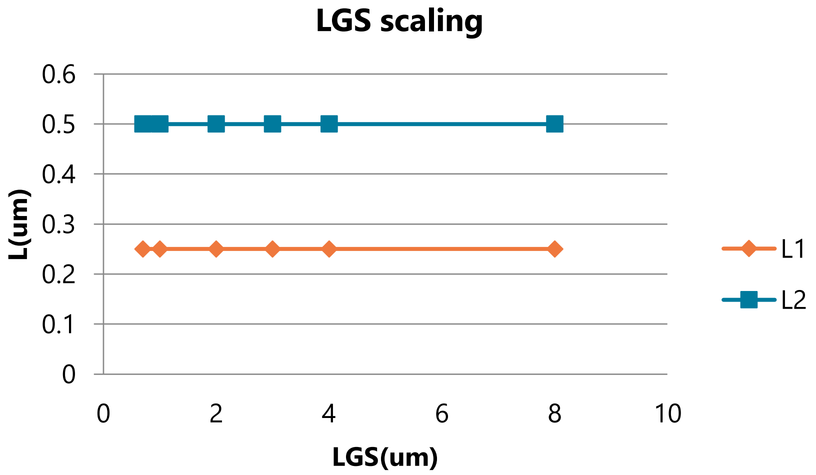
2 Length scaling



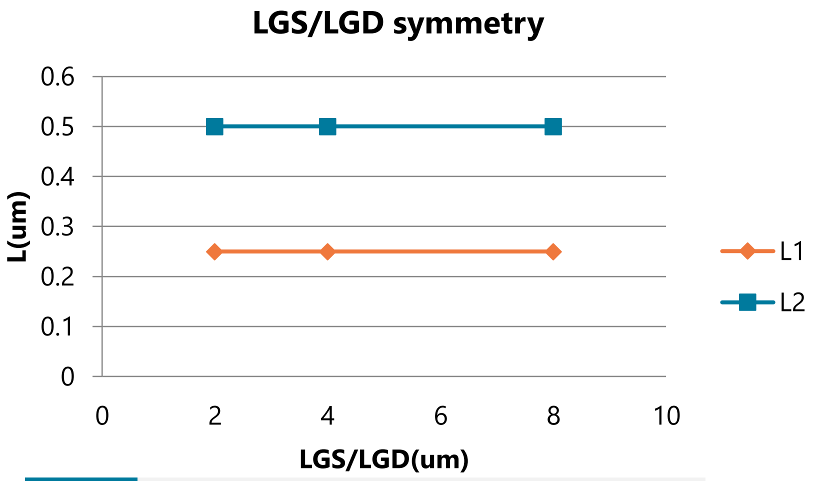
3 LGD scaling



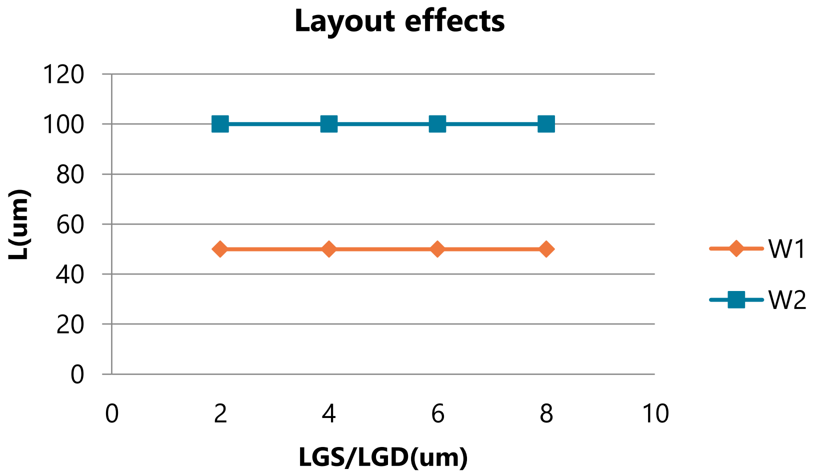
4 LGS scaling



5 LGS/LGD symmetry



6 Layout effects



Reference DUT extraction

Device geometry: L = 250nm; $W_f = 10u; n_f = 2; W_{tot} = 20u$

DC extraction – linear conditions

1. Fitting the linear VD condition parameters:

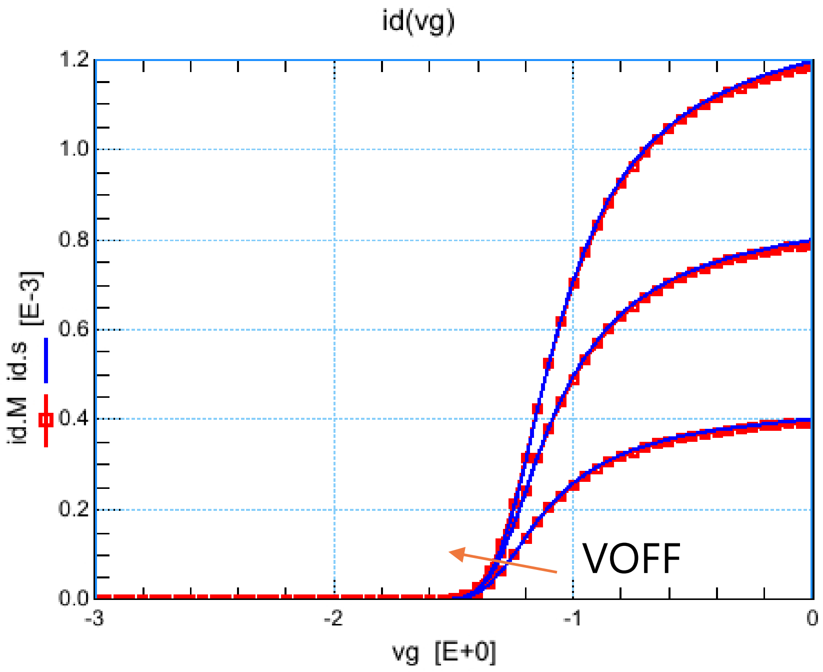
Device geometry: $W_f = 10u; n_f = 2; W_{tot} = 20u$

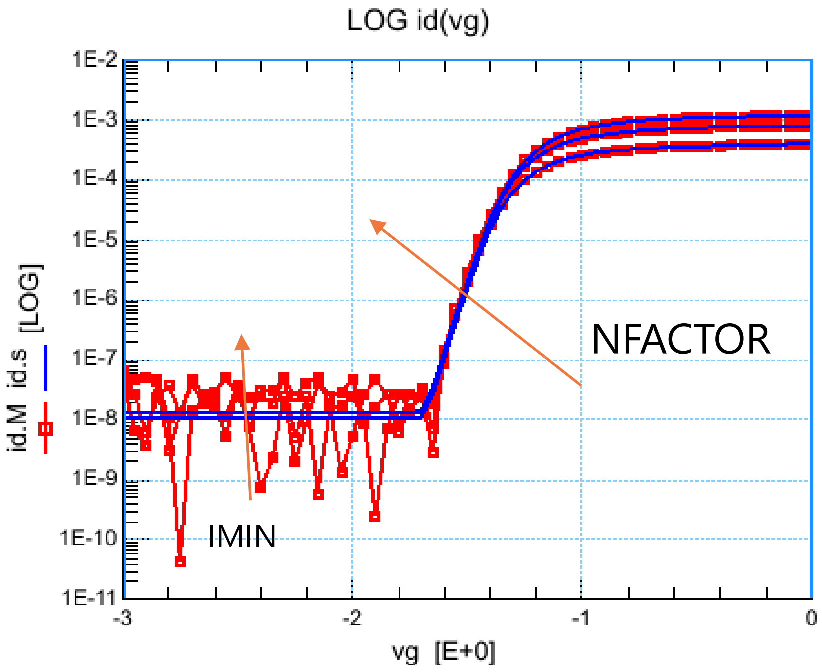
› Extract the parameters such: Cut-off Voltage, Sub-VOFF Slope parameters, low-field mobility and mobility vertical field dependence parameters.

Transfer characteristics:

Measurement conditions :

- VGS range $= -3 < V_{GS} < 0$
- VDS values $= (50,100,150)mV$





Observation :

- *A very good agreement was obtained with id(vg) in linear and log scale.*

DC extraction – linear conditions

2. Checking gm and gm2:

Transfer characteristics:

Device geometry: $W_f = 10u; n_f = 2; W_{tot} = 20u$

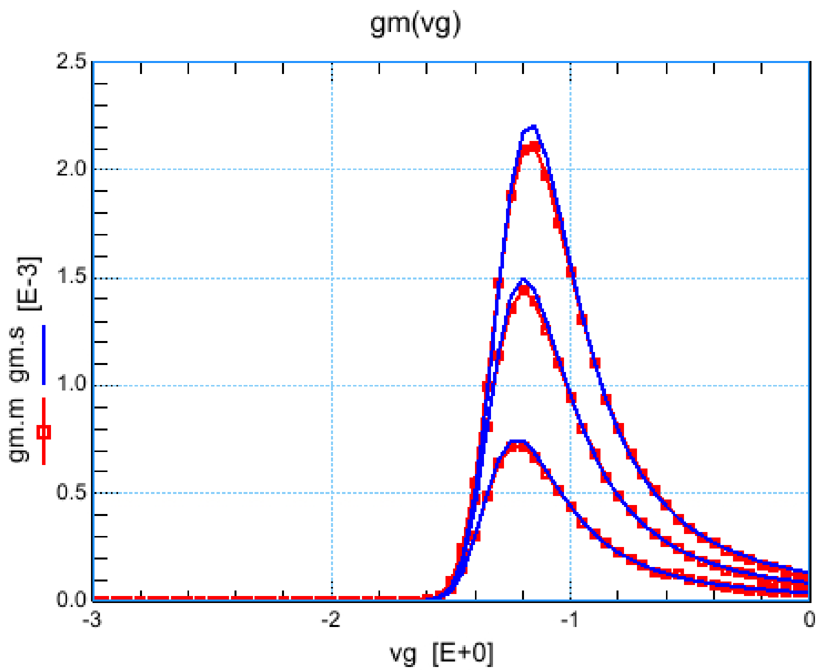
Measurement conditions :

- VGS range $= -3 < V_{GS} < 0$
- VDS values $= (50{,}100{,}150)mV$

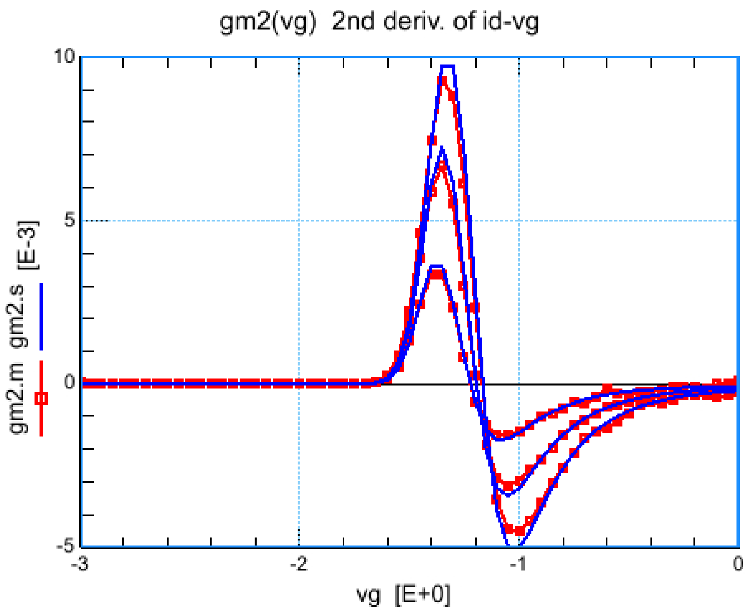
$$\mu_{\mathrm{eff}} = \frac{\mathbf{U_0}(T)}{1 + \mathbf{UA}.E_{y,eff} + \mathbf{UB}.E_{y,eff}^2}$$

Observation :

- *A very good agreement was obtained with gm and gm2.*



$$gm = \frac{\partial I_{DS}}{\partial V_{GS}}$$



$$gm_2 = \frac{\partial^2 I_{DS}}{\partial V_{GS}^2}$$

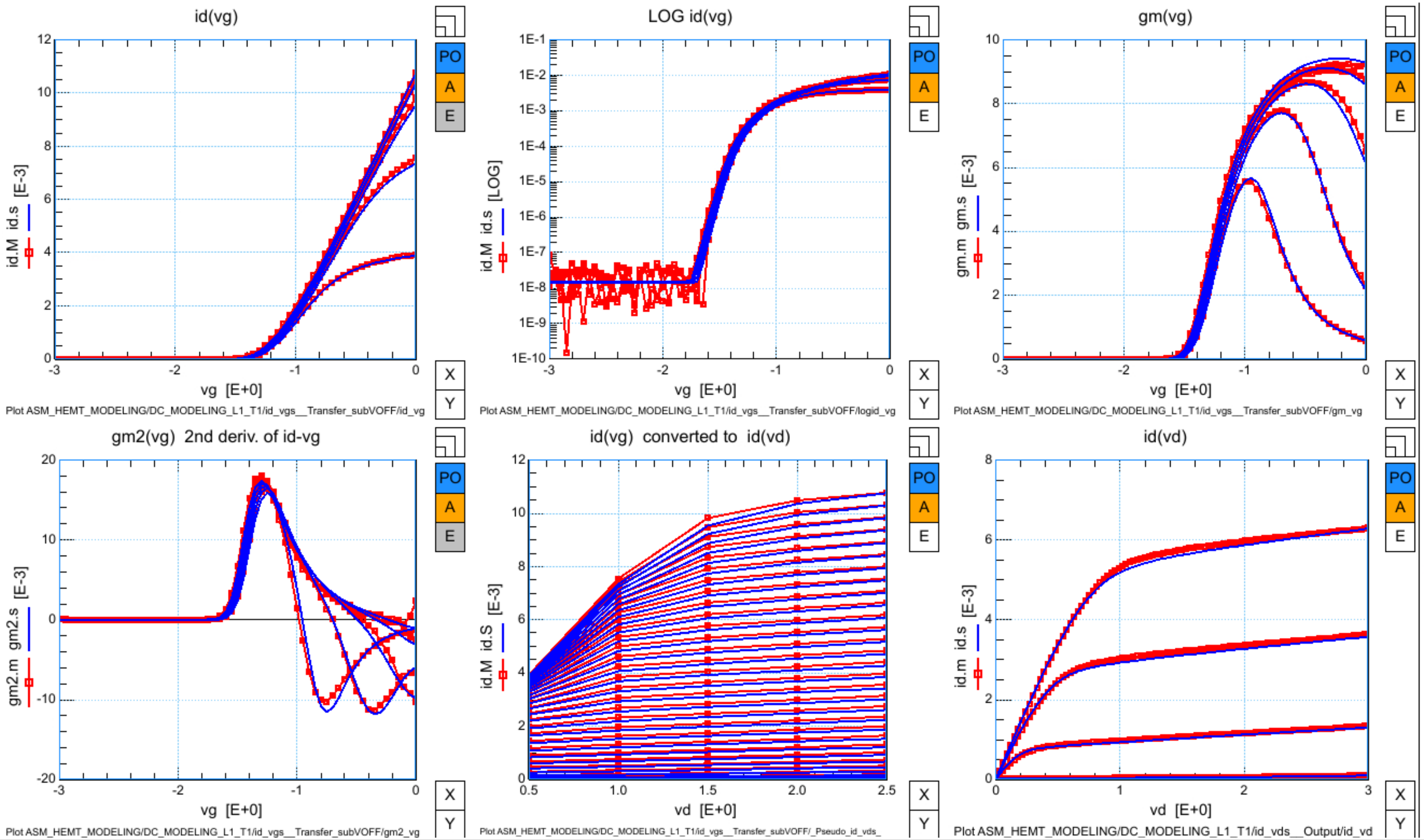
DC extraction – Saturation conditions

Transfer/Output characteristics:

Device geometry: $W_f = 10u; n_f = 2; W_{tot} = 20u$

Measurement conditions:

- ❑ ID – VGS
  - VGS range $= -3 < V_{GS} < 0$
  - VDS values $= (0.5, 1, 1.5, 2, 2.5)V$
- ❑ IDS – VDS
  - VDS range $= 0 < V_{DS} < 3$
  - VGS values $= -2 < V_{GS} < -0.5$



Reference DUT extraction

Capacitances results

CV extraction – VGoff

Device geometry: $W_f = 10u; n_f = 2; W_{tot} = 20u$

CGS/CGD/CDS :

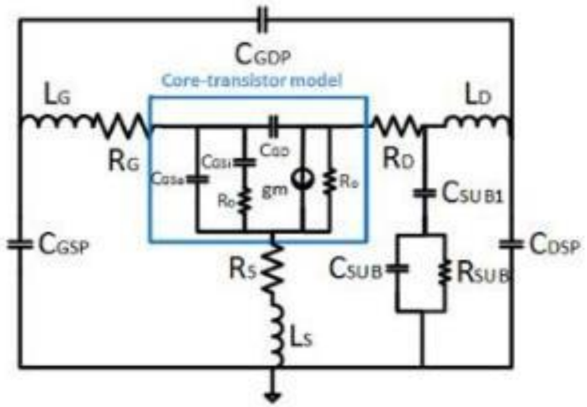
- The model already predicts the intrinsic region device capacitances via its core formulation

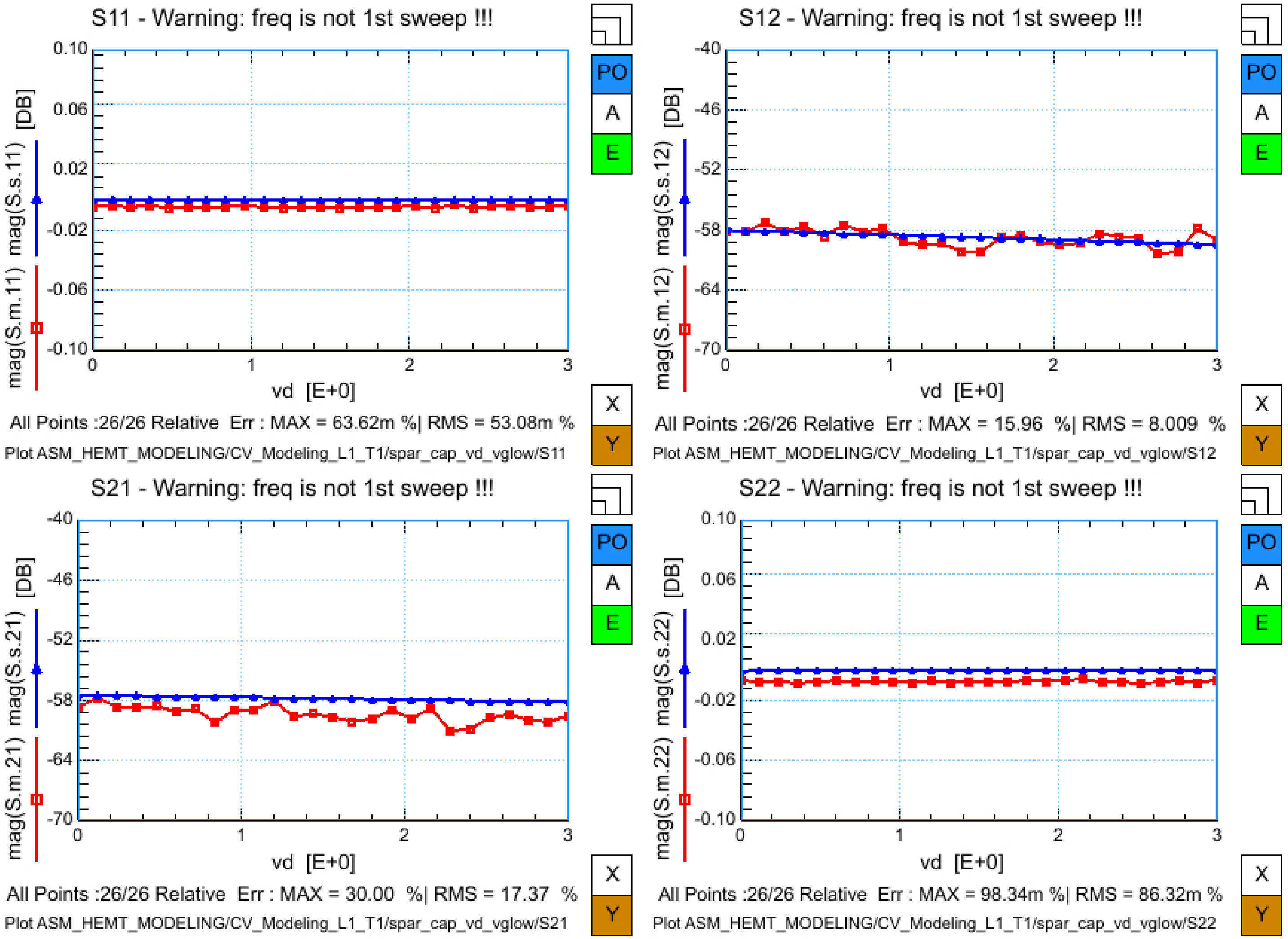
Measurement conditions:

- ❑ $S - \text{param measurements:}$
- $\text{VGS value} = -2.4\ V$
- $\text{VDS range} = 0 < V_{DS} < 3$
- $\text{Frequency} = 100M$

Observation :

- Very good agreement was obtained up to 3V of VDS .





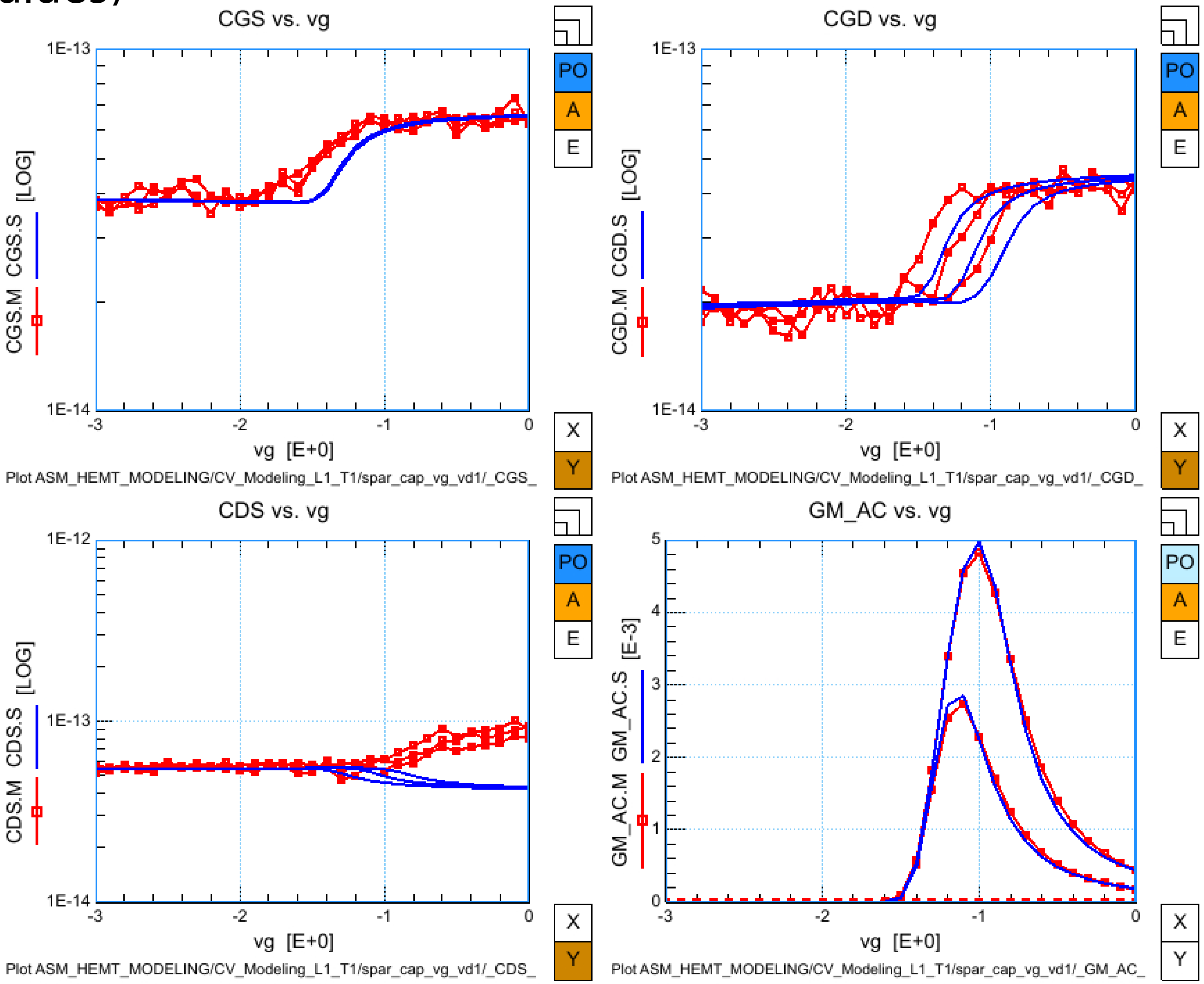
CV extraction – VG Sweep – VD low

$C_{GS}/C_{GD}/C_{DS}$ vs VG (for different VD values)

Device geometry: $W_f = 10u; n_f = 2; W_{tot} = 20u$

Measurement conditions:

- ❑ S – param measurements:
- VGS range $= -3 < V_{GS} < 0$
- VDS range $= 0 < V_{DS} < 400m$
- Frequency $= 100M$



Observation :

- Good agreement was obtained.
- Shift in V_{TH} between Cap/DC
- Incorrect C_{DS} behavior @ On-state

Reference DUT extraction

S-parameters

SP extraction – Freq/VG/VD Sweep

measurements performed up to 67 GHz

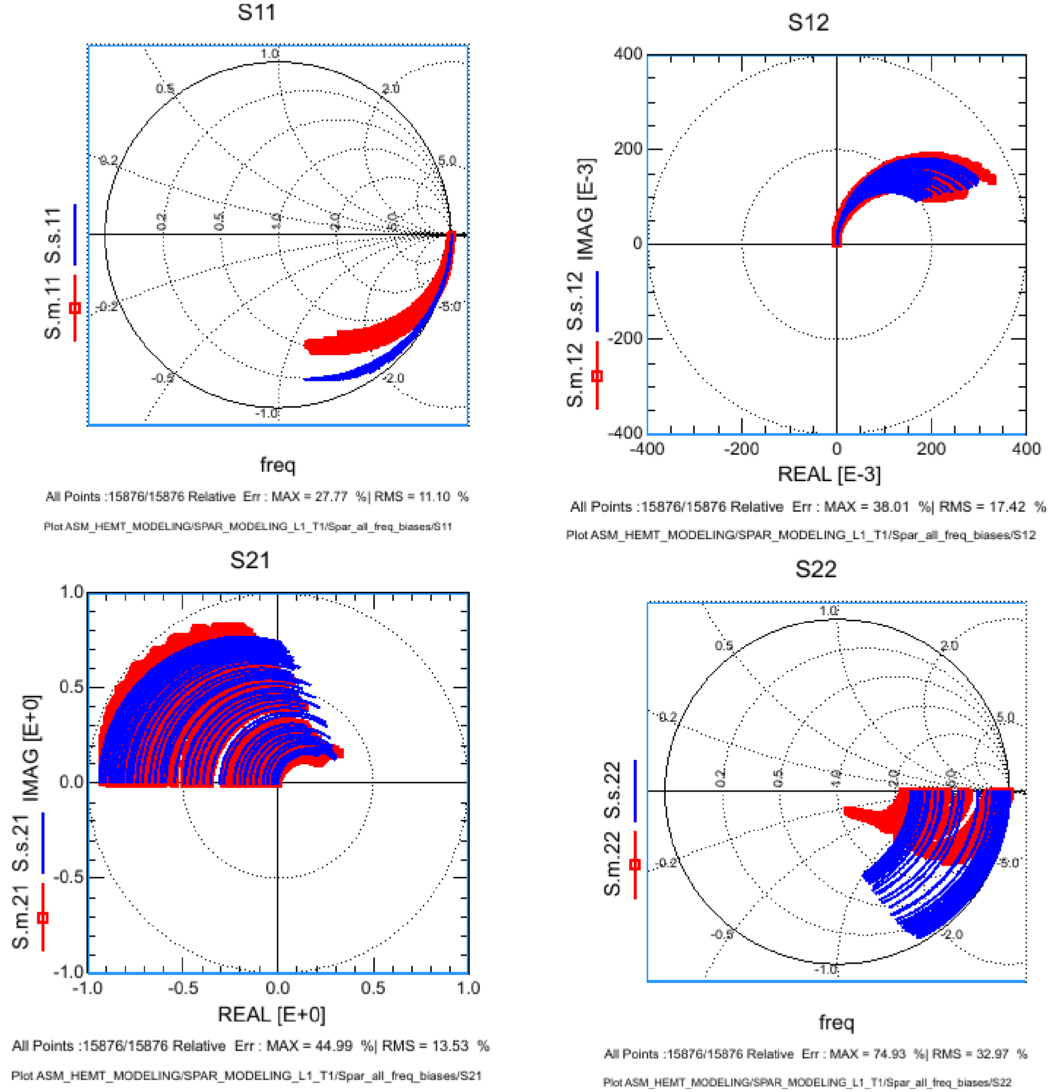
$S_{11}/S_{12}/S_{21}/S_{22}$

Measurement conditions:

- ❑ S – param measurements:
- VGS range = $-3 < V_{GS} < 0$
- VDS range = $0 < V_{DS} < 3$
- Frequency = 100M < F < 25.1G

Observation :

- Very good agreement was obtained for S12/S22.
- Fairly agreement for S21.
- Poor fit for S22



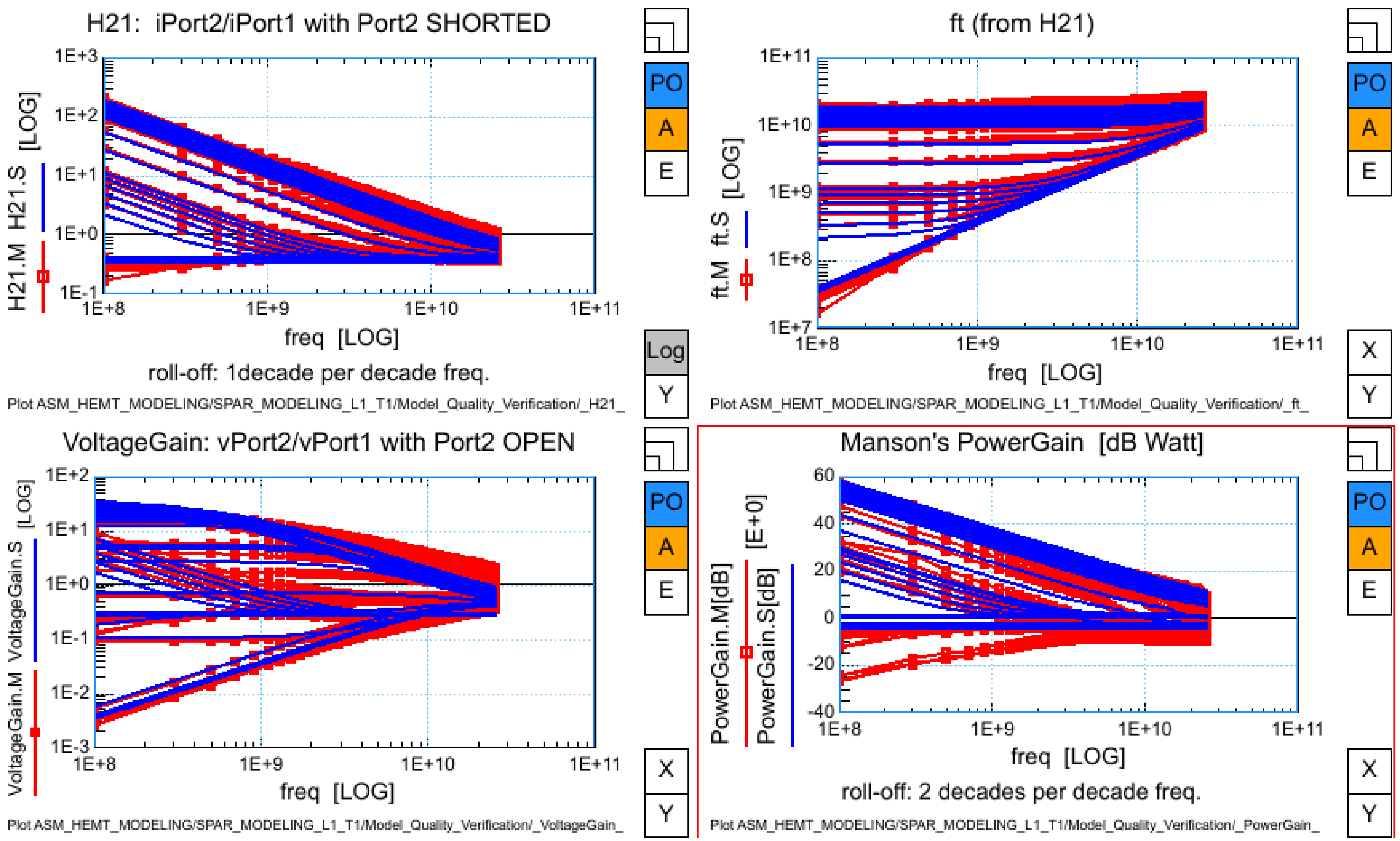
Device geometry: $W_f = 10u; n_f = 2; W_{tot} = 20u$

SP extraction – RF characteristics

$Device\ geometry: W_f = 10u; n_f = 2; W_{tot} = 20u$

Measurement conditions:

- ❑ S − param measurements:
- VGS range $= -3 < V_{GS} < 0$
- VDS range $= 0 < V_{DS} < 3$
- Frequency $= 100M < F < 25.1G$



$$Voltage\ Gain = \frac{v_{port_2}}{v_{port_1}} @ i_{port_2} = 0$$

$$= G_{21} = \frac{1}{H_{21}} = \frac{g_m}{g_{ds}}$$

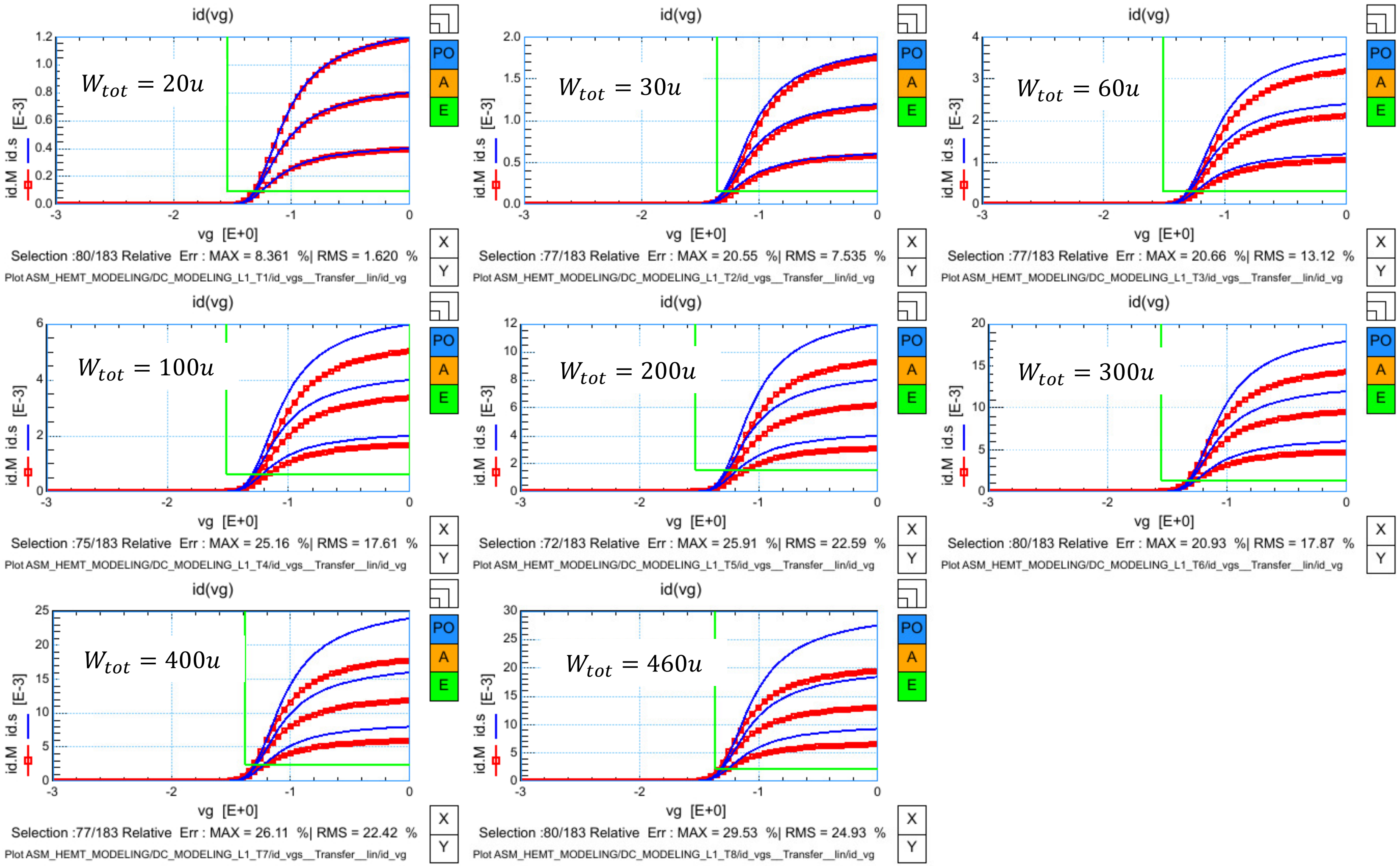
Width Scaling

DC Initial model

Width Scaling – Transfer characteristics – *Before Implementation*

Transfer characteristics:
Linear conditions

Device geometries: "$10u < W_f < 230u$" $\rightarrow$ $n_f = 2$ $\rightarrow$ "$20u < W_{tot} < 460u$"



Measurement conditions :

- VGS range = $-3 < V_{GS} < 0$
- VDS values = $(50,100,150)mV$

Observation :

- *A discrepancy between measurements and simulations begins with an increase in the gate width.*

Width Scaling – Transfer characteristics – *Before Implementation*

Device geometries: "$10u < W_f < 230u$" $\rightarrow$ $n_f = 2$ $\rightarrow$ "$20u < W_{tot} < 460u$"

Transfer characteristics: Linear conditions

Measurement conditions :

- VGS range $= -3 < V_{GS} < 0$
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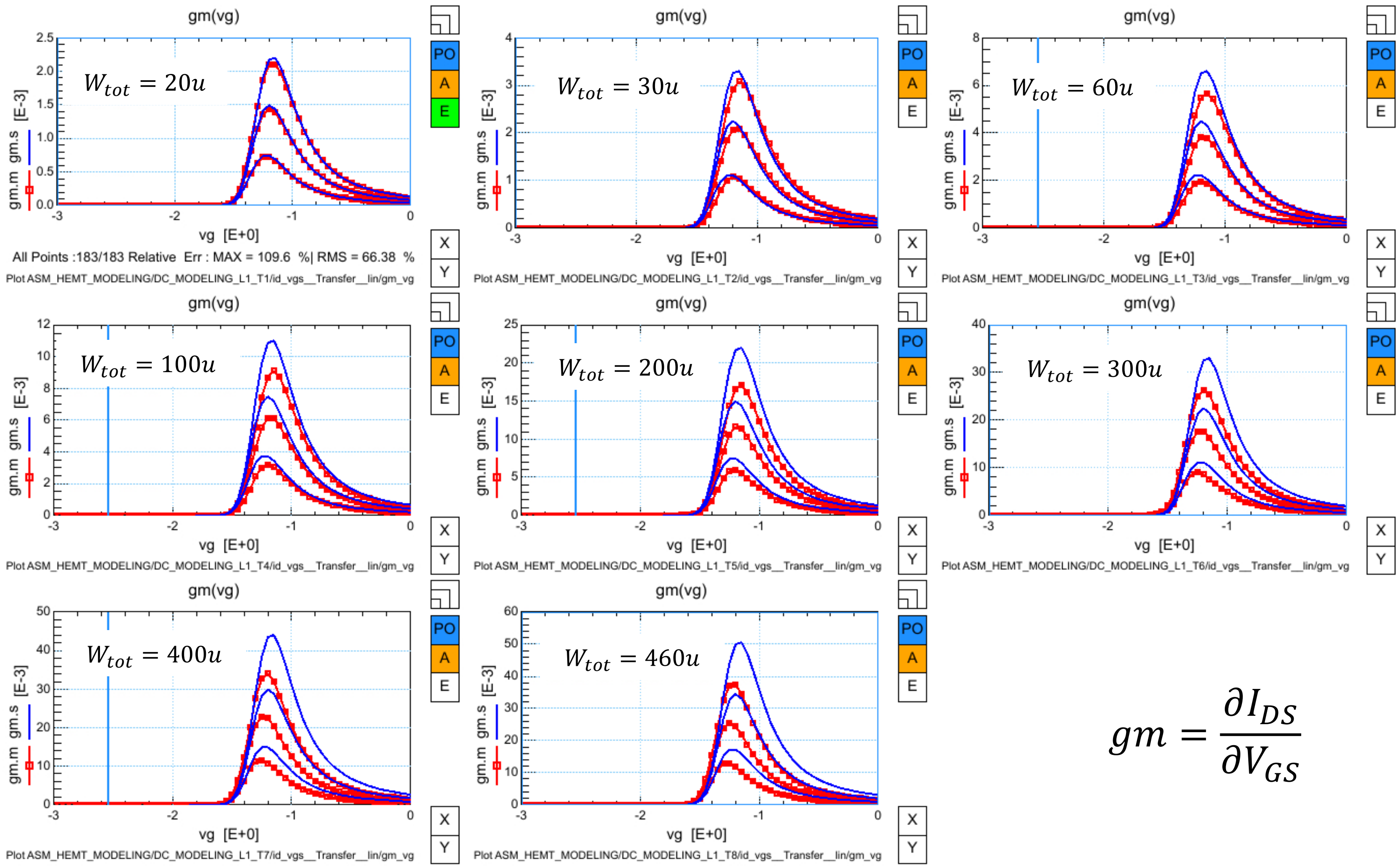


$$gm = \frac{\partial I_{DS}}{\partial V_{GS}}$$

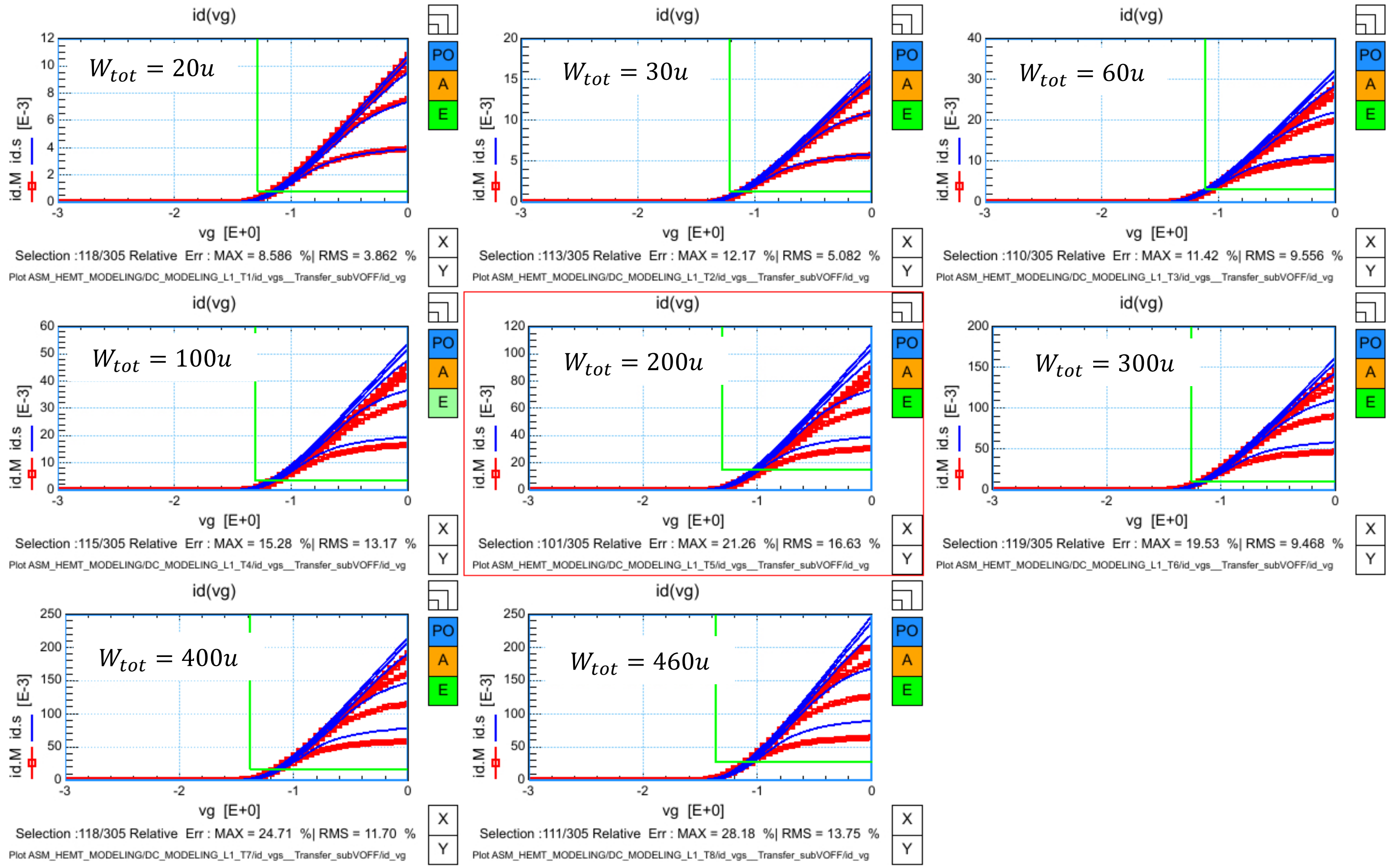
Width Scaling – Transfer characteristics – *Before Implementation*

Device geometries: "$10u < W_f < 230u$" $\rightarrow$ $n_f = 2$ $\rightarrow$ "$20u < W_{tot} < 460u$"

Transfer characteristics: Saturation conditions

Measurement conditions:

- ❑ ID – VGS
- VGS range = $-3 < V_{GS} < 0$
- VDS values = $(0.5,1,1.5,2,2.5)V$



Observation :

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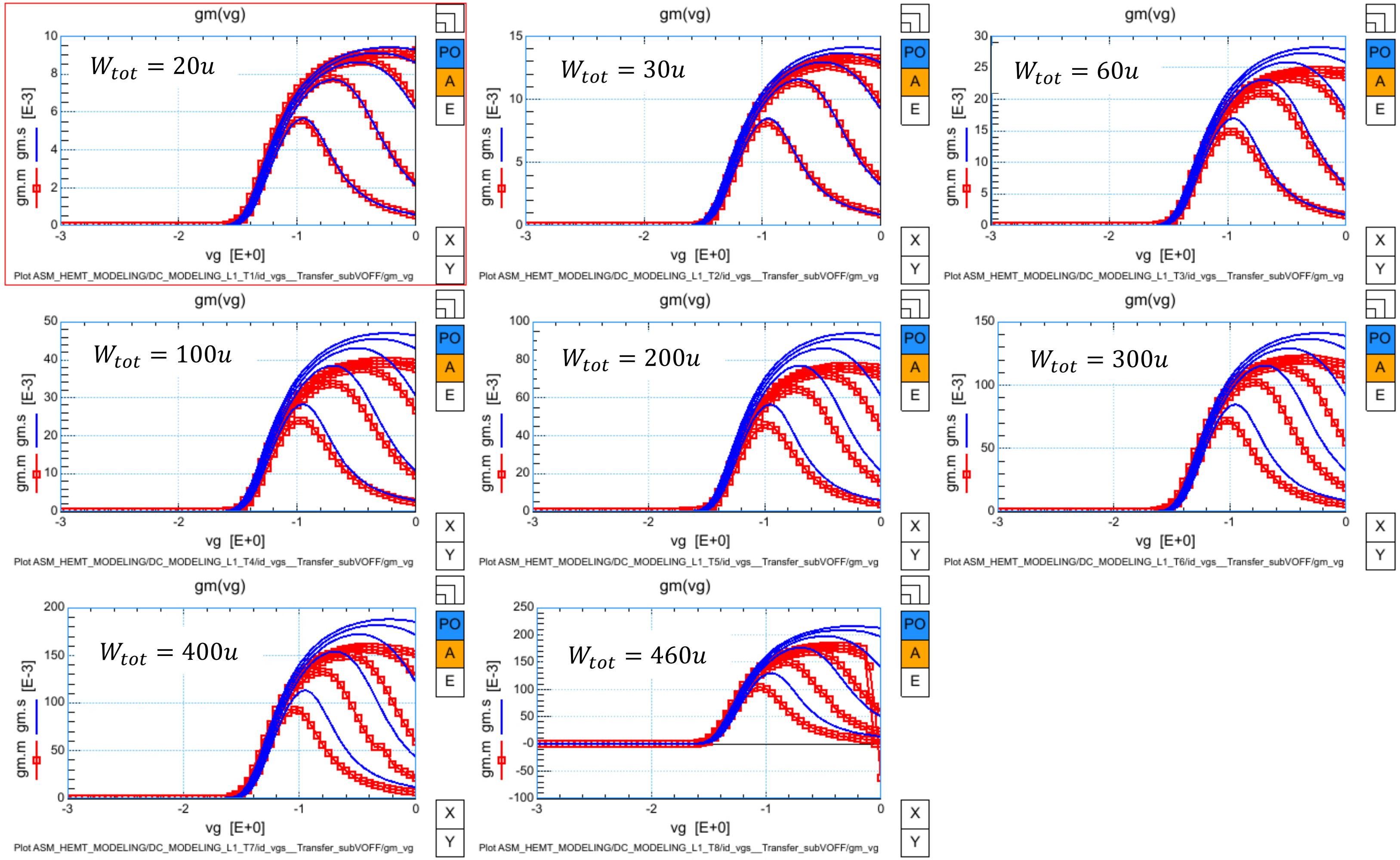
Width Scaling – Transfer characteristics – *Before Implementation*

Device geometries: $"10u < W_f < 230u" \rightarrow n_f = 2 \rightarrow "20u < W_{tot} < 460u"$

Transfer characteristics: Saturation conditions

Measurement conditions:

- ❑ ID – VGS
- VGS range $= -3 < V_{GS} < 0$
- VDS values $= (0.5, 1, 1.5, 2, 2.5)V$



Observation :

- *A discrepancy between measurements and simulations begins with an increase in the gate width.*

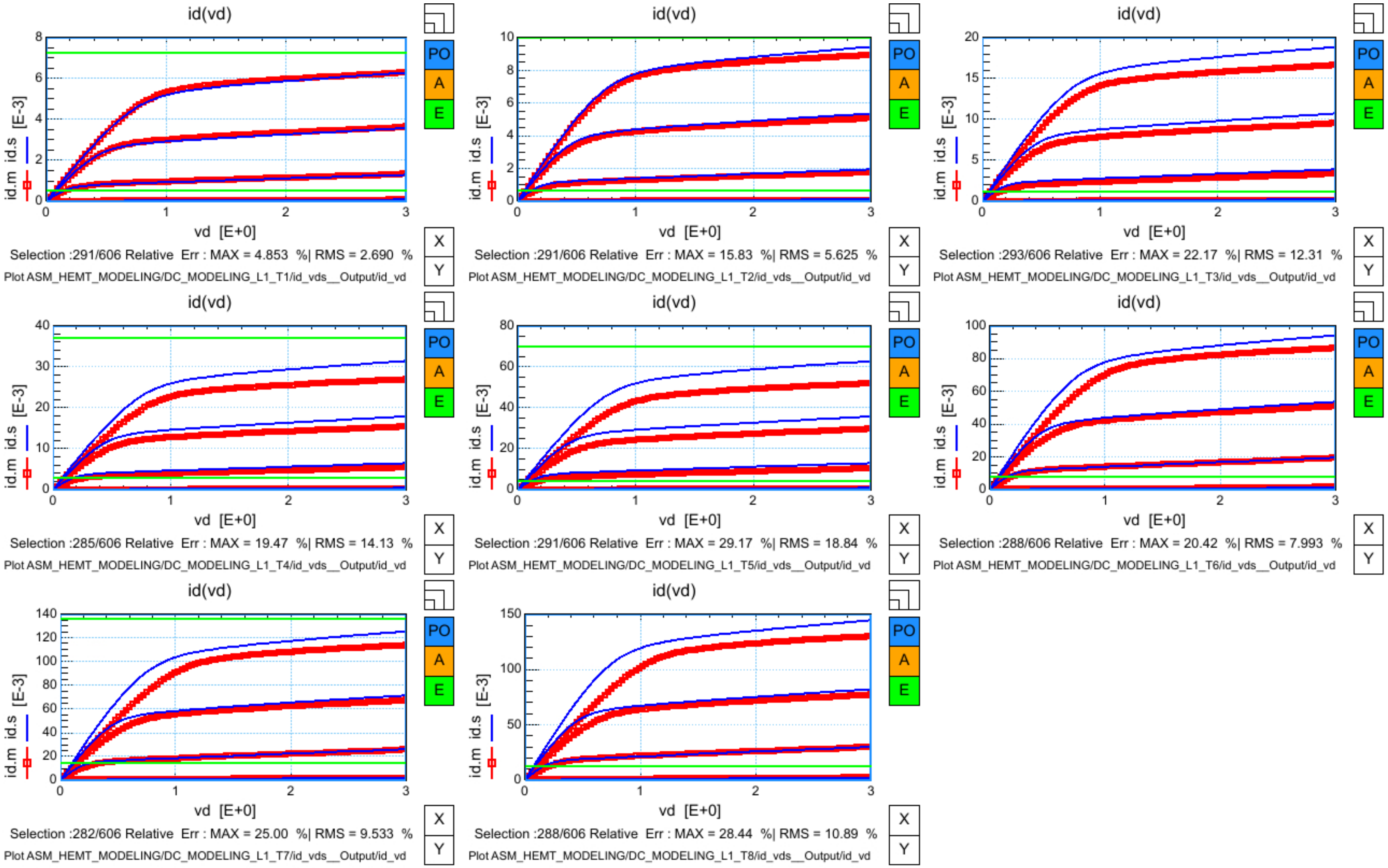
Width Scaling – Output characteristics – *Before Implementation*

Output characteristics:

Device geometries: $"10u < W_f < 230u" \rightarrow n_f = 2 \rightarrow "20u < W_{tot} < 460u"$

Measurement conditions:

- ❑ ID – VGS
  - VGS range $= -3 < V_{GS} < 0$
  - VDS values $= (0.5, 1, 1.5, 2, 2.5)V$
- ❑ IDS – VDS
  - VDS range $= 0 < V_{DS} < 3$
  - VGS values $= -2 < V_{GS} < -0.5$



Observation :

- *A discrepancy between measurements and simulations begins with an increase in the gate width.*

Scaling rules

Development

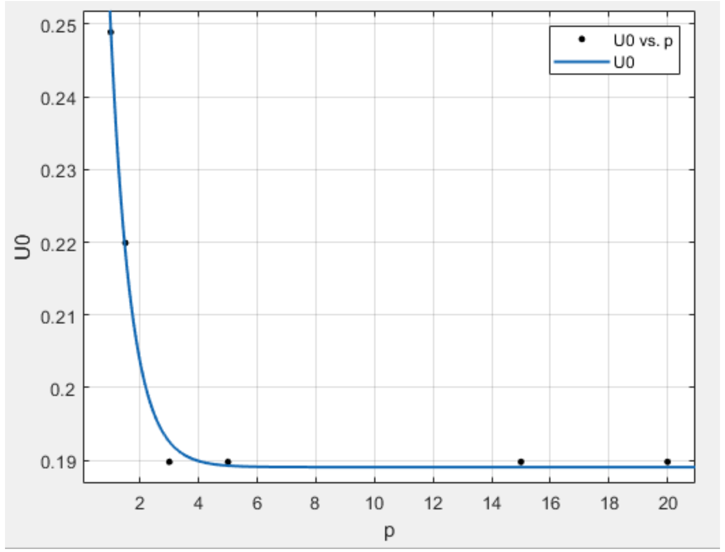
Scaling rules development

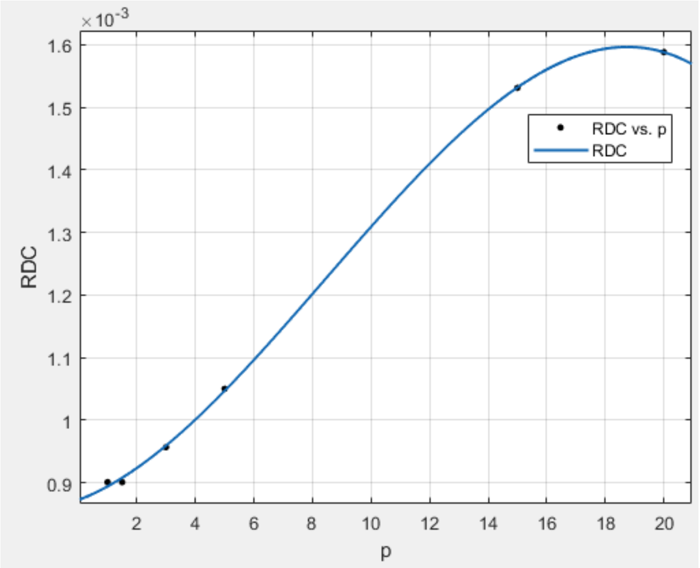
Scaling rules that depend on the form of variation of the model parameter:

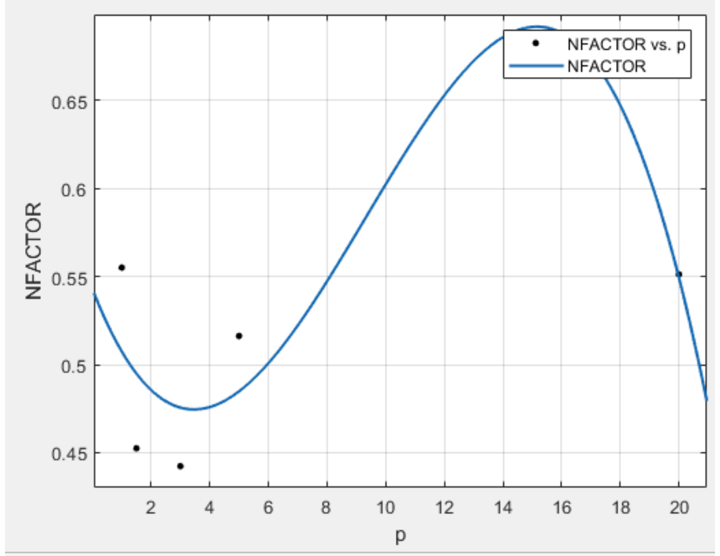
$$U_{O_s} = A.\exp\left(-B * \frac{w}{w_N}\right)^{\alpha}$$

$$R_{DC} = \sum_{i=0}^{3} a_i \left(\frac{w}{w_N}\right)^{i}$$

$$N_{factor} = \sum_{i=0}^{3} a_i \left(\frac{w}{w_N}\right)^{i}$$







Trying to reach high R^2

Table of Fits

Fit na...	Data	Fit type	SSE	R-square	DFE	Adj R-sq	RMSE	# Coeff
NFACT...	NFACTOR...	poly3	0.0062	0.8428	2	0.6070	0.0556	4
RDC	RDC vs. p	poly3	1.1303e-10	0.9998	2	0.9994	7.5178e-06	4
U0	U0 vs. p	a*exp(-b*...	1.0754e-05	0.9965	3	0.9942	0.0019	3
UA	UA vs. p	power2	2.0510e-17	0.4820	3	0.1367	2.6147e-09	3
UB	UB vs. p	poly3	4.3690e-33	0.8929	2	0.7321	4.6739e-17	4
VOFF	VOFF vs. p	poly2	1.9036e-04	0.7975	3	0.6625	0.0080	3

$@w_N = 20\mu m$

Verilog-A implementation

xfab

- *A new macros section has been introduced in the vacode*

```
/////////// List Of Geometry Scaling Parameters //////////
    `MPRco( wN          ,10.0e-6     ,"m"        ,1e-9     ,inf      ," Normalized Channel Width" )
    `MPRoo( U0_C1       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility C1 - Width Scaling" )
    `MPRoo( U0_C2       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility C2 - Width Scaling" )
    `MPRoo( U0_C3       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility C3 - Width Scaling" )
    `MPRoo( rdc_C1      ,0           ,"-"        ,-inf     ,inf      ," RDC C1 - Width Scaling" )
    `MPRoo( rdc_C2      ,0           ,"-"        ,-inf     ,inf      ," RDC C2 - Width Scaling" )
    `MPRoo( rdc_C3      ,0           ,"-"        ,-inf     ,inf      ," RDC C3 - Width Scaling" )
    `MPRoo( rdc_C4      ,0           ,"-"        ,-inf     ,inf      ," RDC C4 - Width Scaling" )
    `MPRoo( voff_C1     ,0           ,"-"        ,-inf     ,inf      ," voff C1 - Width Scaling" )
    `MPRoo( voff_C2     ,0           ,"-"        ,-inf     ,inf      ," voff C2 - Width Scaling" )
    `MPRoo( voff_C3     ,0           ,"-"        ,-inf     ,inf      ," voff C3 - Width Scaling" )
    `MPRoo( UA_C1       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility - Coeff- C1 - Width Scaling" )
    `MPRoo( UA_C2       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility - Coeff- C2 - Width Scaling" )
    `MPRoo( UA_C3       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility - Coeff- C3 - Width Scaling" )
    `MPRoo( UB_C1       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility - Coeff2- C1 - Width Scaling" )
    `MPRoo( UB_C2       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility - Coeff2- C2 - Width Scaling" )
    `MPRoo( UB_C3       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility - Coeff2- C3 - Width Scaling" )
    `MPRoo( UB_C4       ,0           ,"-"        ,-inf     ,inf      ," Low field mobility - Coeff2- C4 - Width Scaling" )
    `MPRoo( NFA_C1      ,0           ,"-"        ,-inf     ,inf      ," nfactor C1 - Width Scaling" )
    `MPRoo( NFA_C2      ,0           ,"-"        ,-inf     ,inf      ," nfactor C2 - Width Scaling" )
    `MPRoo( NFA_C3      ,0           ,"-"        ,-inf     ,inf      ," nfactor C3 - Width Scaling" )
    `MPRoo( NFA_C4      ,0           ,"-"        ,-inf     ,inf      ," nfactor C4 - Width Scaling" )
```

- *Updated model equations:*

$$\mu_{\text{eff}} = \frac{\mathbf{U_0}(T)}{1 + \mathbf{UA}.E_{y,eff} + \mathbf{UB}.E_{y,eff}^2} \longrightarrow \mu_{\text{eff}} = \frac{\mathbf{U_{0s}}(T)}{1 + \mathbf{UAs}.E_{y,eff} + \mathbf{UBs}.E_{y,eff}^2}$$

```
/////////// Function for PSID Calculation - Width Scaling //////////
`define PSID_S(Tdev,Tnom,epsilon,delta,beta,ALPHAN,ALPHAD,Vtv,Cch,U0val,ute,VSATval,at,Cg,psis,Vg0,ua,ub,l,Vds,GAMMA0Ival, GAMMA1Ival,
mulf_tdev,Vdeff,psid,w,wN,U0_C1,U0_C2,U0_C3,UA_C1,UA_C2,UA_C3,UB_C1,UB_C2,UB_C3,UB_C4) \
U0val_s    = U0_C1*exp(-U0_C2*(w/wN))+U0_C3; \
mulf_tdev = U0val_s*pow((Tdev/Tnom),ute); \
vsat_tdev = VSATval*pow((Tdev/Tnom),at); \
t0         = (Cg/epsilon)*abs(Vg0 - psis); \
ua_s       = UA_C1*pow((w/wN),UA_C2)+UA_C3; \
ub_s       = UB_C1*pow((w/wN),3) + UB_C2*pow((w/wN),2) + UB_C3*(w/wN) + UB_C4; \
mu_eff     = mulf_tdev/(1.0 + ua_s*(t0) + ub_s*t0*t0); \
t0         = 2.0*vsat_tdev/mu_eff; \
t1         = 0.5*Vg0 + 0.5*sqrt(Vg0*Vg0 + 4.0*`ep_psi*`ep_psi); \
Vdsat      = t0*l*t1/(t0*l + t1 ); \
```

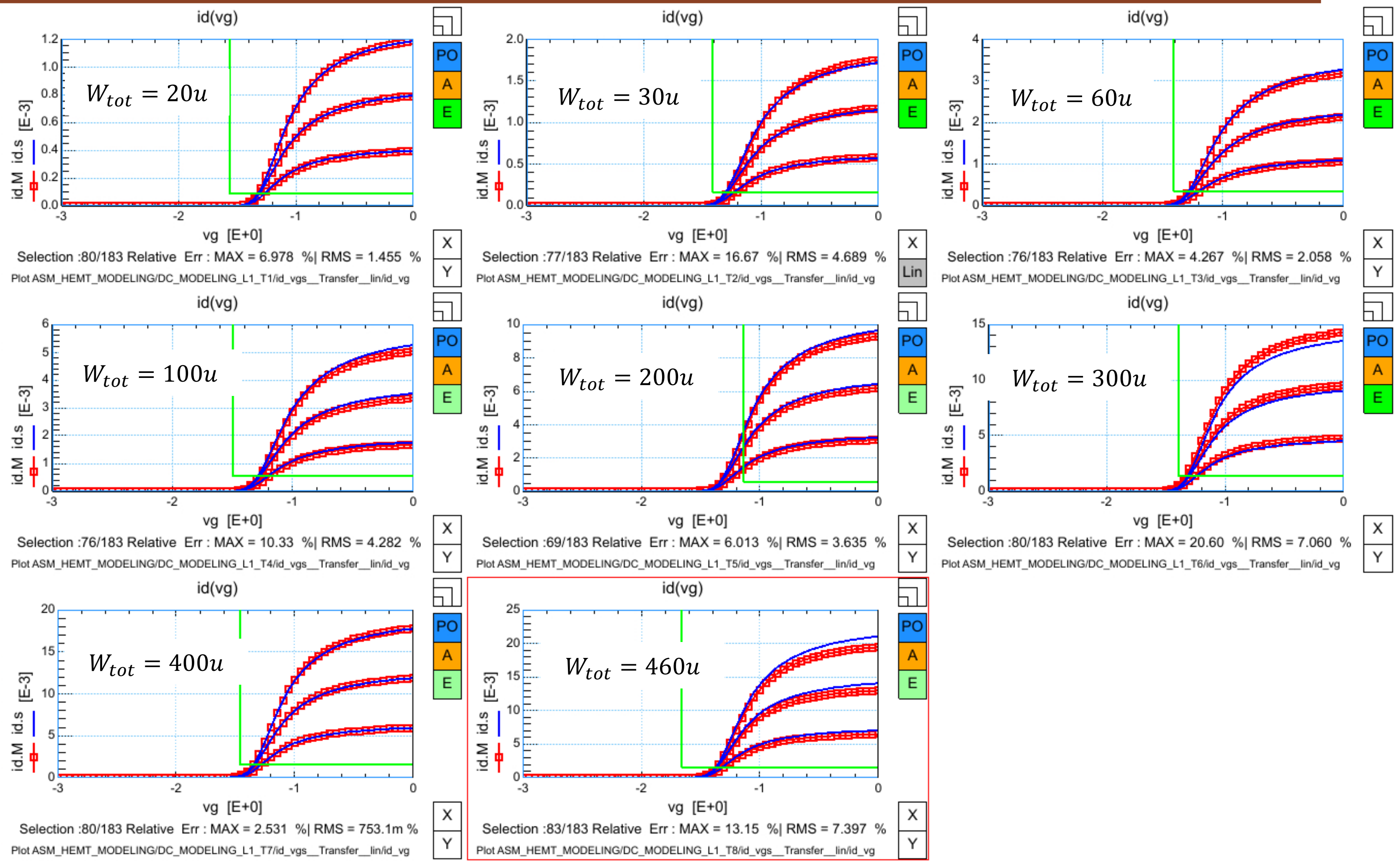
Width Scaling

Results/DC

Width Scaling – Transfer characteristics – *After Implementation*

Transfer characteristics: Linear conditions

Device geometries: "$10u < W_f < 230u$" $\rightarrow n_f = 2 \rightarrow$ "$20u < W_{tot} < 460u$"



Measurement conditions :

- VGS range $= -3 < V_{GS} < 0$
- VDS values $= (50{,}100{,}150)mV$

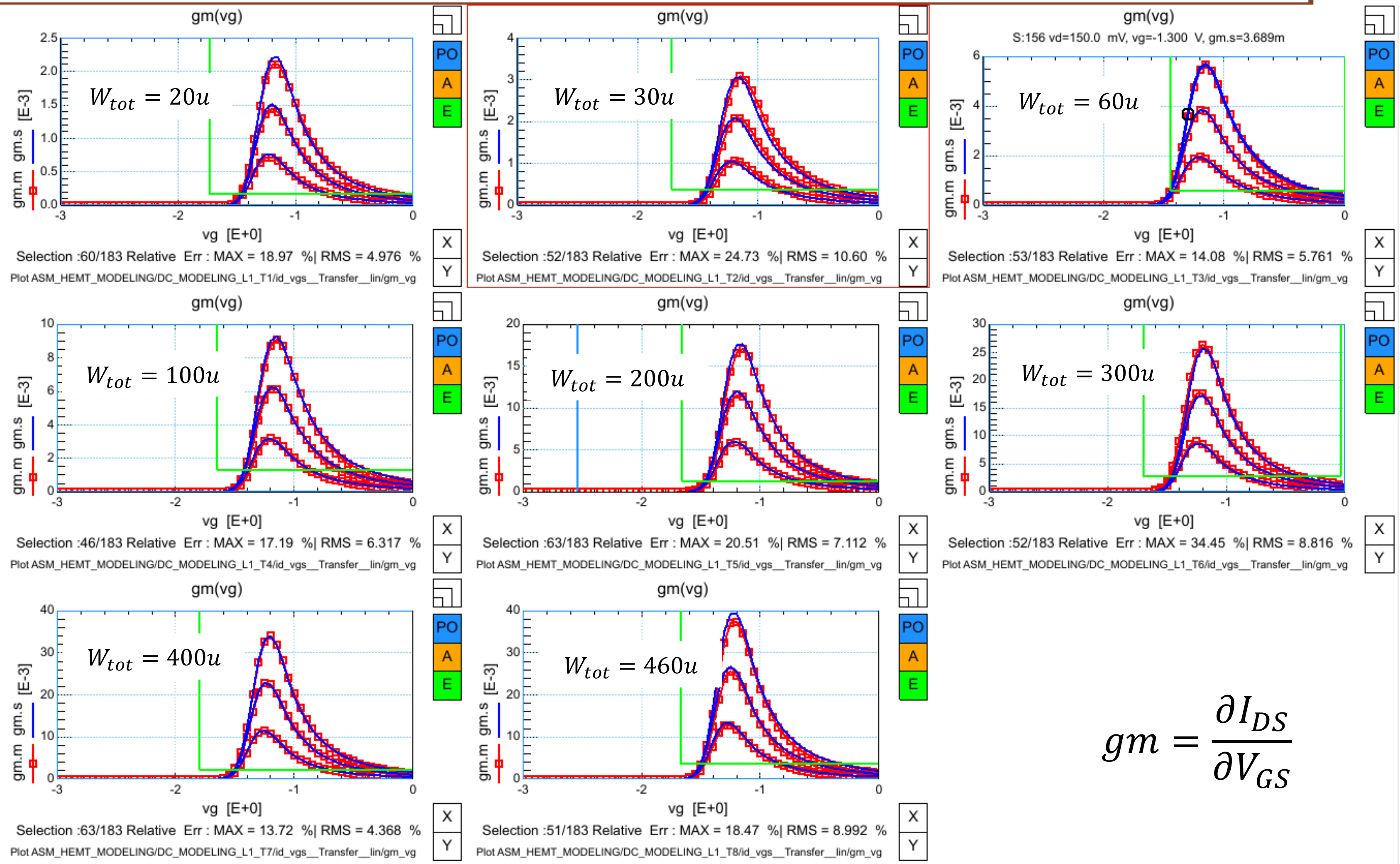
Observation :

- *A very good agreement between measurements and simulations begins with an increase in the gate width.*

Width Scaling – Transfer characteristics – *After Implementation*

Transfer characteristics:
Linear conditions

Device geometries: "$10u < W_f < 230u$" $\rightarrow$ $n_f = 2$ $\rightarrow$ "$20u < W_{tot} < 460u$"



Measurement conditions :

- VGS range $= -3 < V_{GS} < 0$
- VDS values $= (50,100,150)mV$

Observation :

- *A very good agreement between measurements and simulations begins with an increase in the gate width.*

$$gm = \frac{\partial I_{DS}}{\partial V_{GS}}$$

Width Scaling – Transfer characteristics – *After Implementation*

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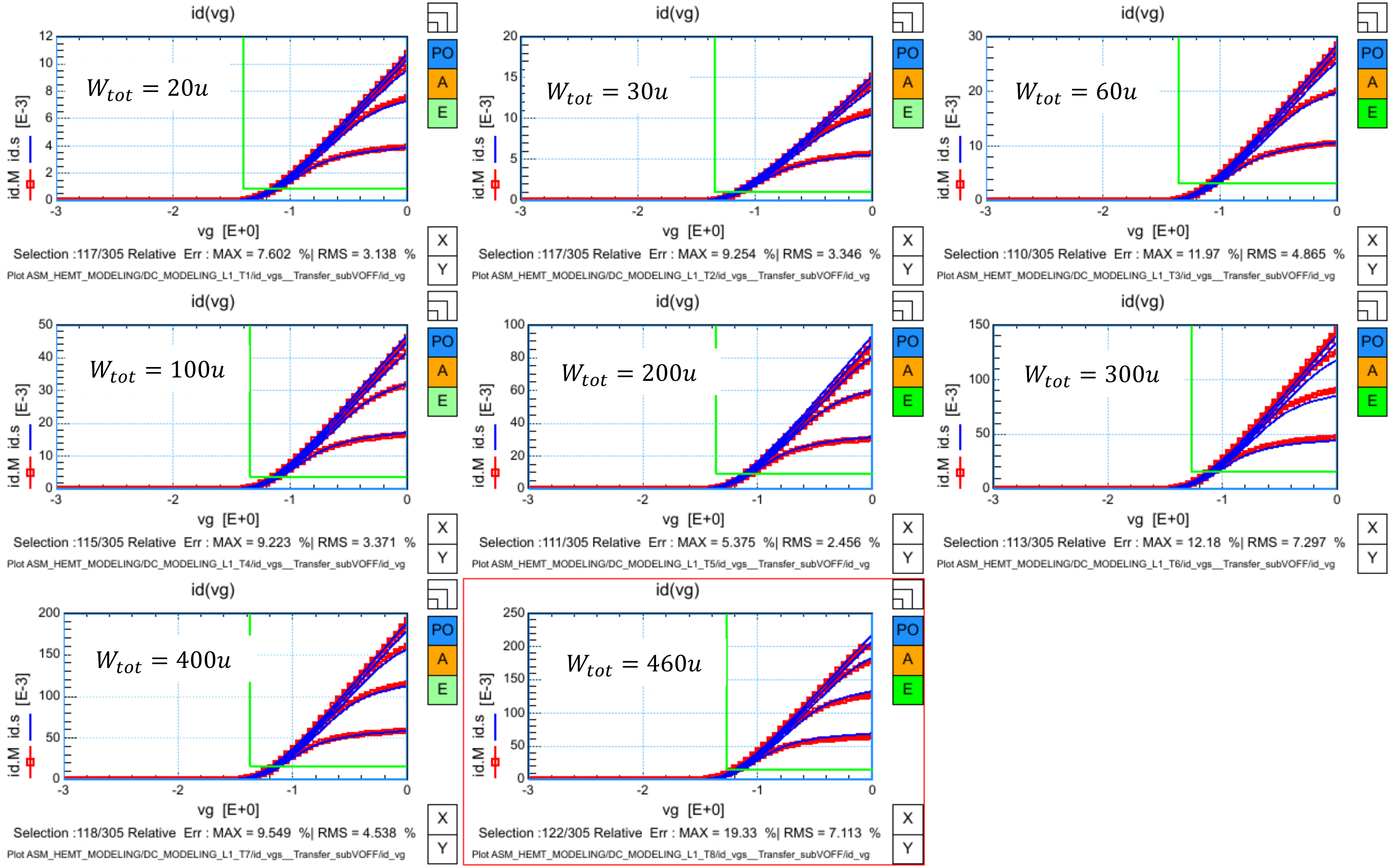
Transfer characteristics: Saturation conditions

Device geometries: $"10u < W_f < 230u" \rightarrow n_f = 2 \rightarrow "20u < W_{tot} < 460u"$

Measurement conditions:

- ID – VGS
- VGS range $= -3 < V_{GS} < 0$
- VDS values $= (0.5,1,1.5,2,2.5)V$



Observation :

- *A very good agreement between measurements and simulations begins with an increase in the gate width.*

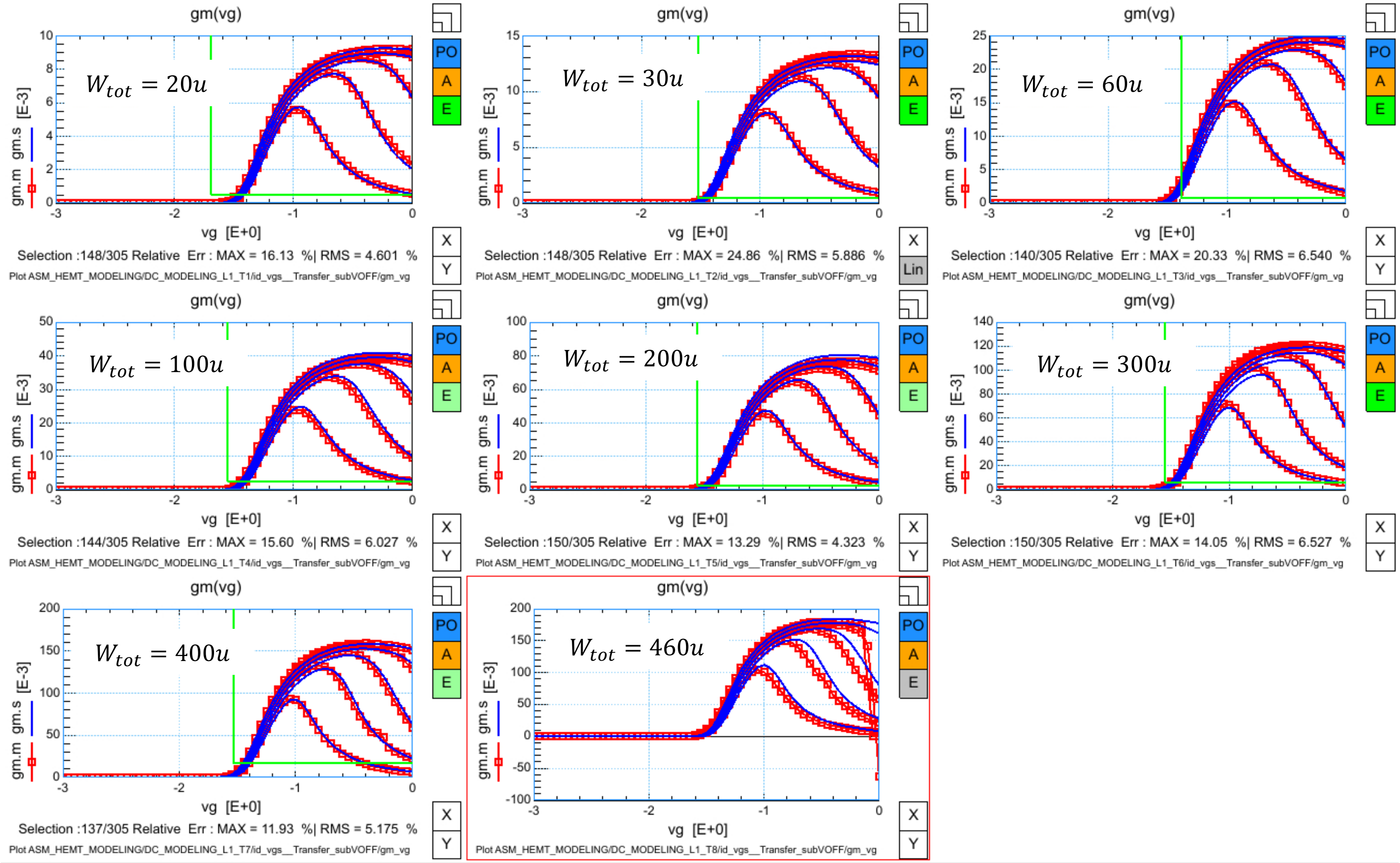
Width Scaling – Transfer characteristics – *After Implementation*

Device geometries: "$10u < W_f < 230u$" $\rightarrow$ $n_f = 2$ $\rightarrow$ "$20u < W_{tot} < 460u$"

Transfer characteristics: Saturation conditions

Measurement conditions:

- ❑ ID – VGS
- VGS range $= -3 < V_{GS} < 0$
- VDS values $= (0.5,1,1.5,2,2.5)V$



Observation :

- *A very good agreement between measurements and simulations begins with an increase in the gate width.*

Width Scaling – Output characteristics – *After Implementation*

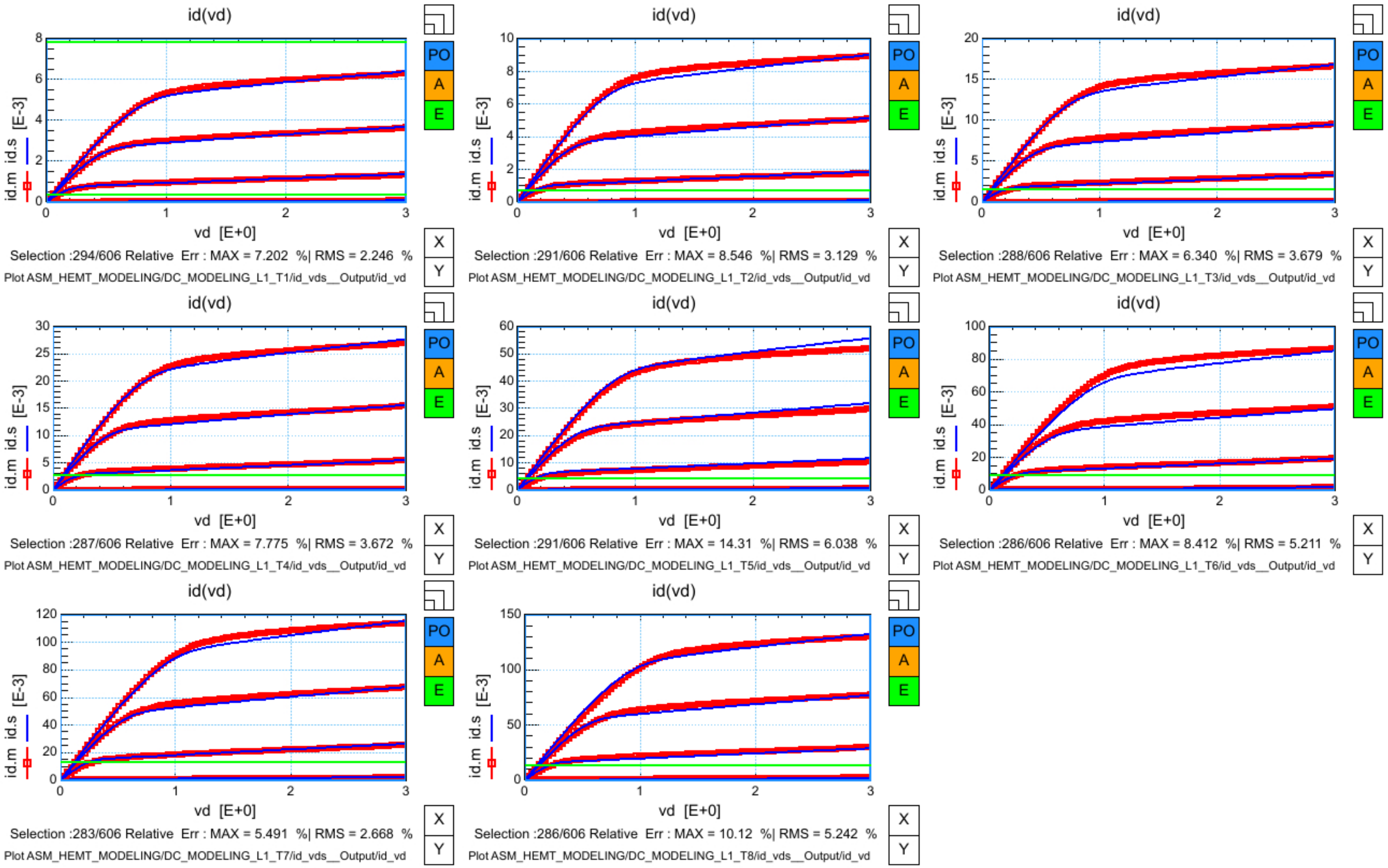
Output characteristics:

Device geometries: "$10u < W_f < 230u$" $\rightarrow$ $n_f = 2$ $\rightarrow$ "$20u < W_{tot} < 460u$"

Measurement conditions:

❑ ID – VGS
- VGS range $= -3 < V_{GS} < 0$
- VDS values $= (0.5,1,1.5,2,2.5)V$

❑ IDS – VDS
- VDS range $= 0 < V_{DS} < 3$
- VGS values $= -2 < V_{GS} < -0.5$



Observation :
- *A very good agreement between measurements and simulations begins with an increase in the gate width.*

on-going work

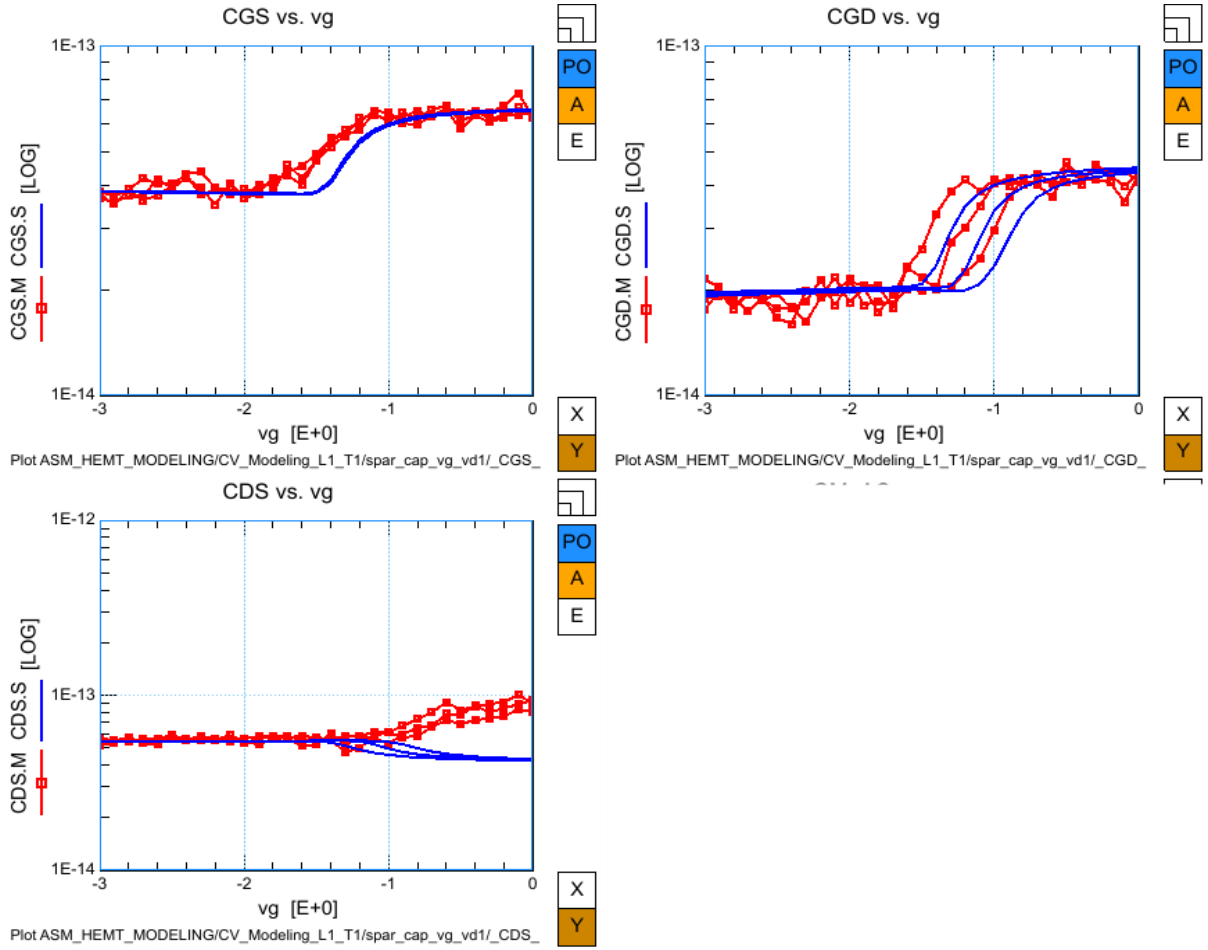
current model weaknesses; width Scaling development for the capacitances

Model weaknesses: reference model vs W-scalable model

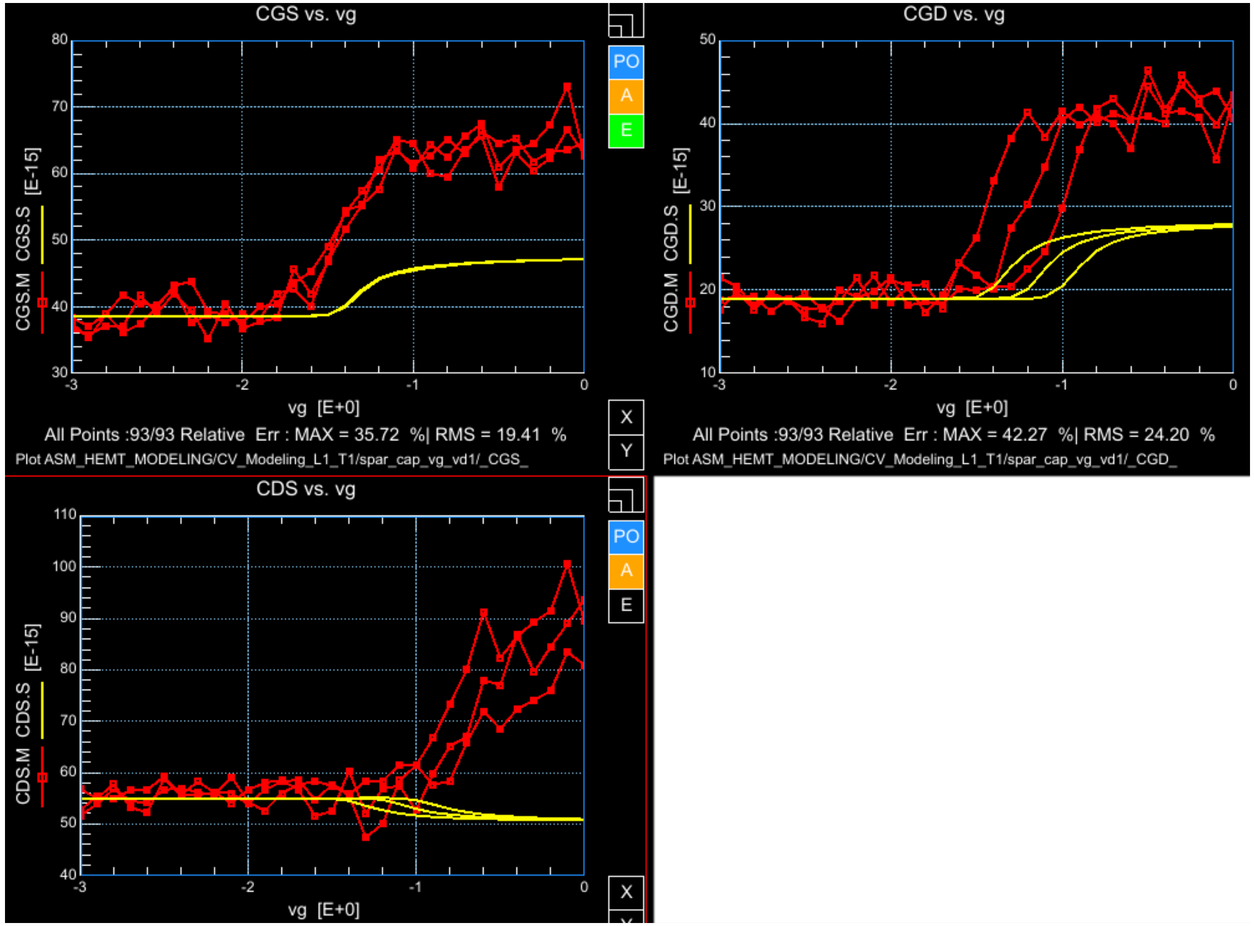
$C_{GS}/C_{GD}/C_{DS}\ vs\ VG$ (for different VD values)

$Device\ geometry{:}\ W_f = 10u; n_f = 2; W_{tot} = 20u$

$Initial\ model\ (fixed\ geometry)$

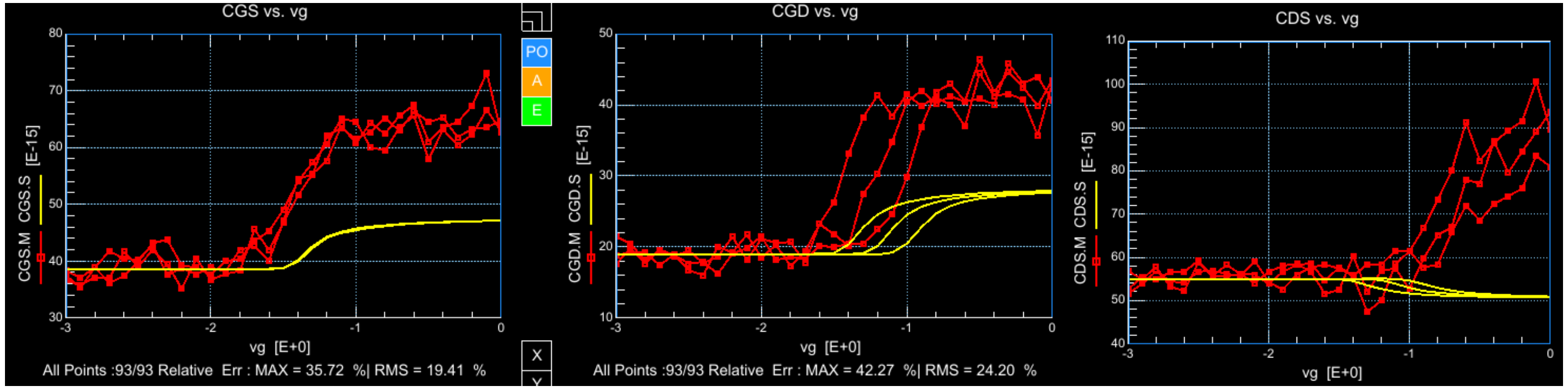


$DC\ \ W - scalable\ model$

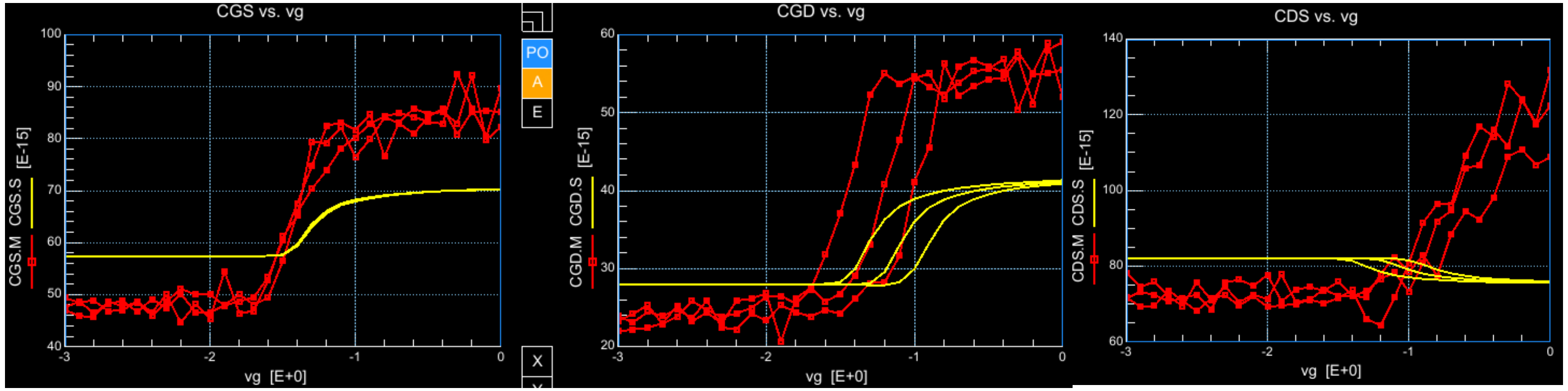


Model weaknesses: W-scaling of the capacitances

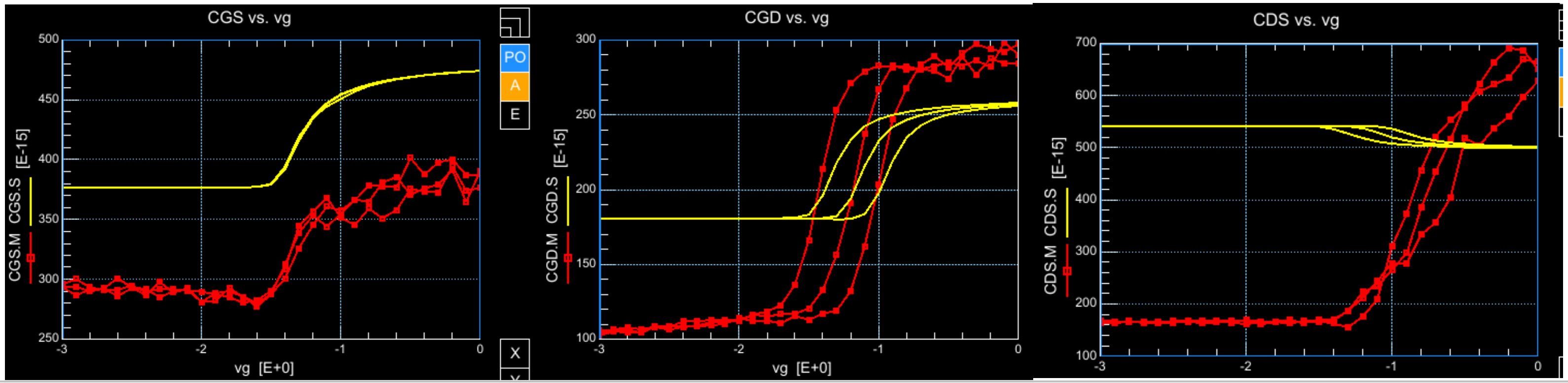
Device geometry:
$W_f = 10u;$
$n_f = 2;$
$W_{tot} = 20u$



Device geometry:
$W_f = 15u;$
$n_f = 2;$
$W_{tot} = 30u$



Device geometry:
$W_f = 100u;$
$n_f = 2;$
$W_{tot} = 200u$



Width Scaling improvement - CV

Summary of parameters used for W-scaling

- Parameters used for DC W-scaling:
  - u0 : " Low field mobility"
  - ua : " Mobility Degradation coefficient first order"
  - ub : " Mobility Degradation coefficient second order"
  - rdc : " Drain Contact Resistance"
  - voff : " Cut-off voltage"
  - nfactor : " Sub-voff Slope parameters"

- Parameters used for CV W-scaling:
  - cgso : " Gate-source overlap capacitance"
  - cgdo : " Gate-drain overlap capacitance"
  - cdso : " Cds capacitance parameter"

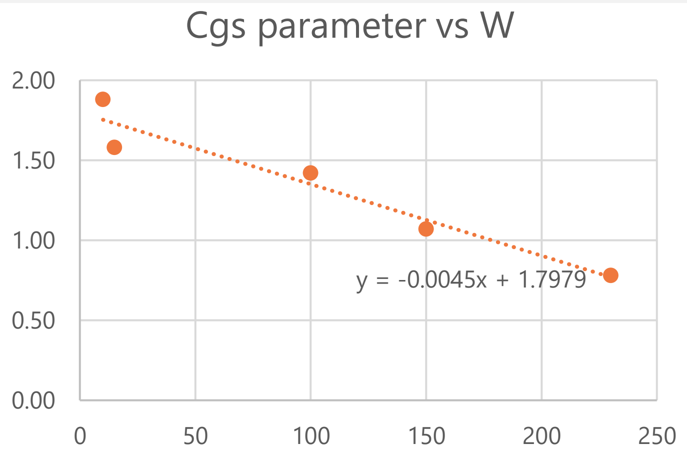
- Examples :

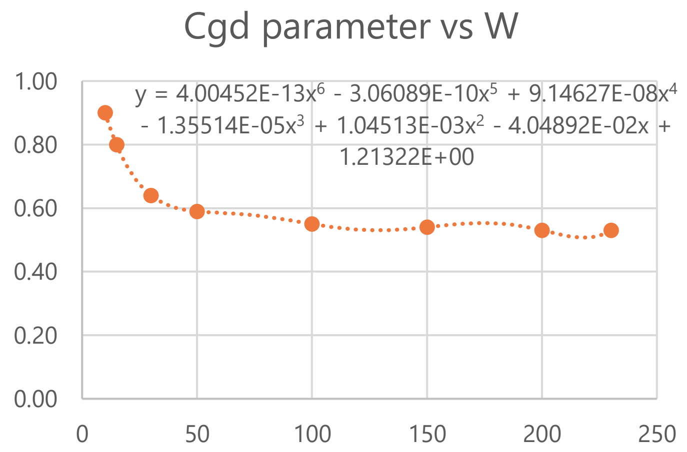
$$\mu_{\mathrm{eff}} = \frac{\mathbf{U_{0s}}(T)}{1 + \mathbf{UAs}.E_{y,eff} + \mathbf{UBs}.E_{y,eff}^2}$$

$$U_{O_s} = A.\exp\left(-B * \frac{w}{w_N}\right)^{\alpha}$$

$$\mathrm{C}_{gs} = \boldsymbol{C_{gs0}} * \mathrm{C}_{gs} * \frac{w}{w_N}$$

$$\boldsymbol{C_{gs0}} = A * \left(\frac{w}{w_N}\right) + \mathrm{B}$$





CV – VG Sweep – VD low --- Proposed CV scalable model - v1

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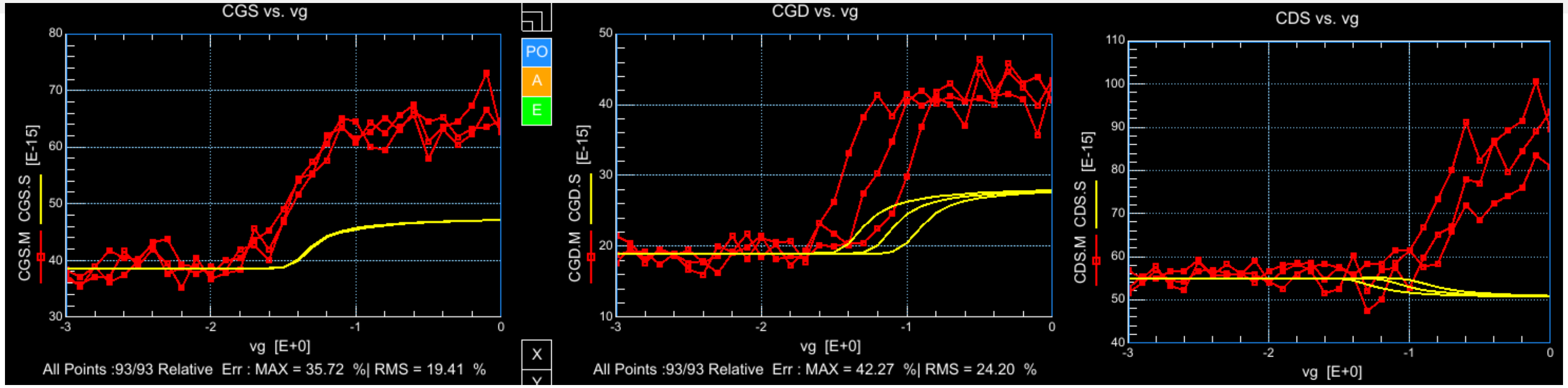
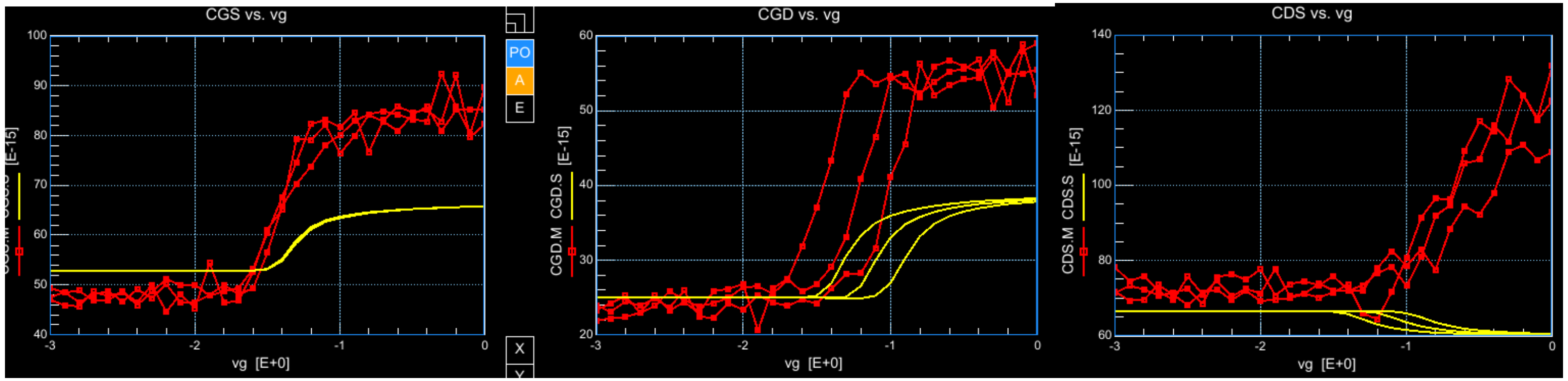
Device geometry:

$$W_f = 10u;$$
$$n_f = 2;$$
$$W_{tot} = 20u$$



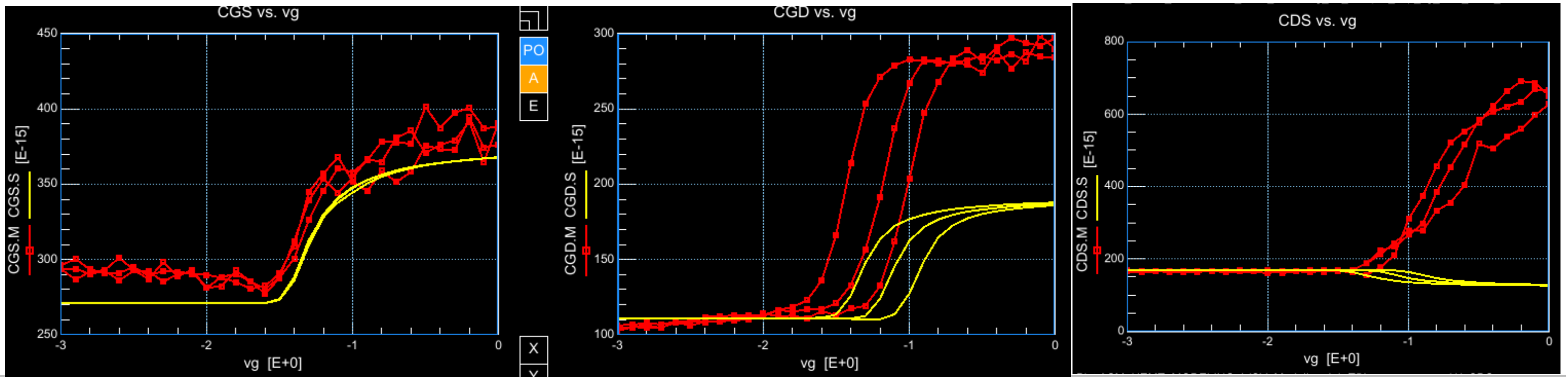
Device geometry:

$$W_f = 15u;$$
$$n_f = 2;$$
$$W_{tot} = 30u$$



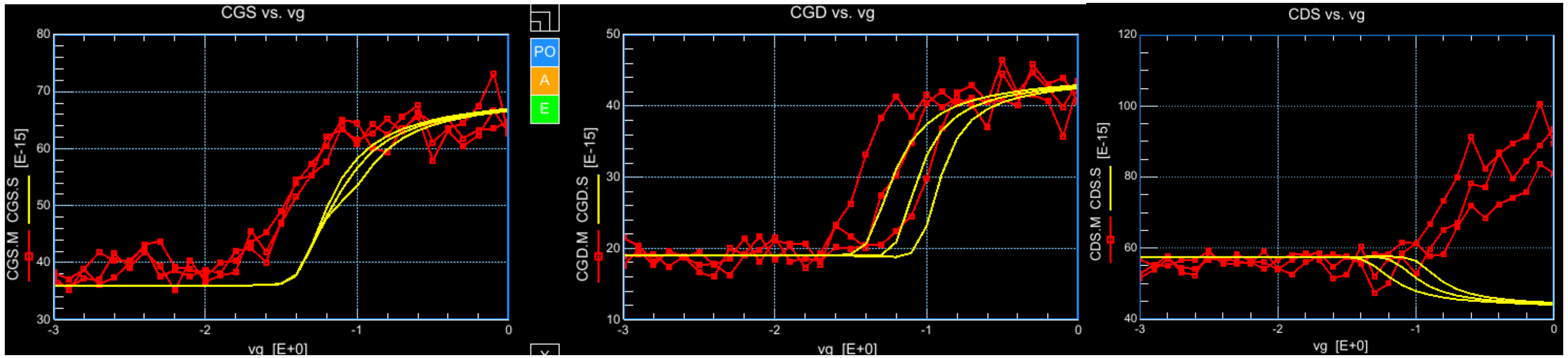
Device geometry:

$$W_f = 100u;$$
$$n_f = 2;$$
$$W_{tot} = 200u$$

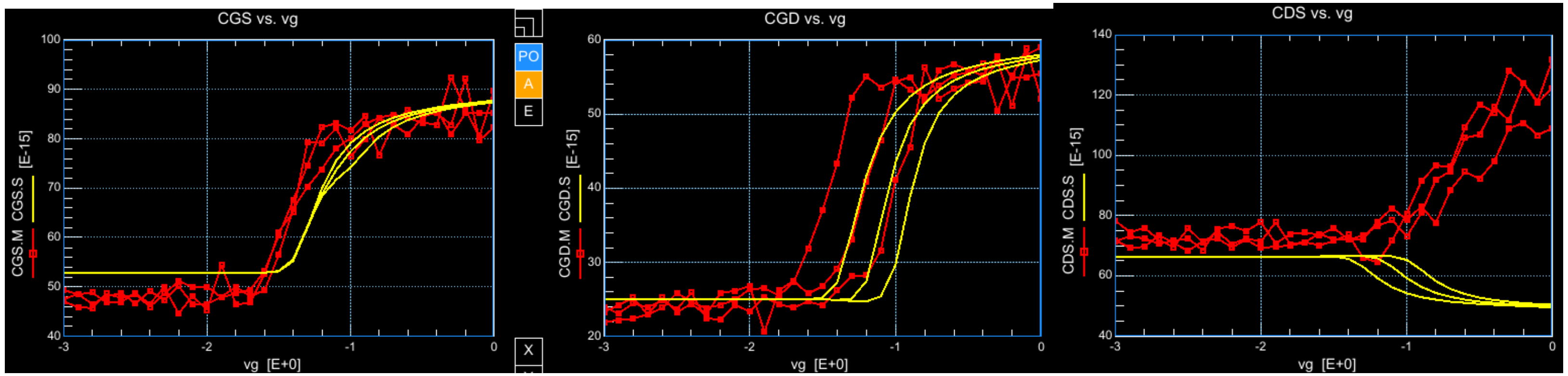


CV – VG Sweep – VD low --- Proposed CV scalable model - v2

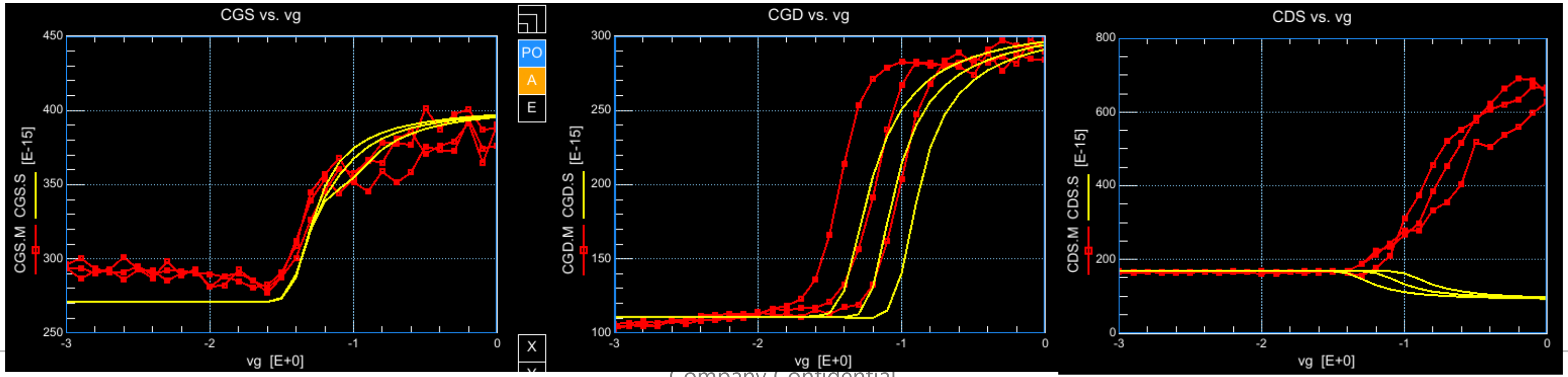
Device geometry:
$$W_f = 10u;$$
$$n_f = 2;$$
$$W_{tot} = 20u$$



Device geometry:
$$W_f = 15u;$$
$$n_f = 2;$$
$$W_{tot} = 30u$$



Device geometry:
$$W_f = 100u;$$
$$n_f = 2;$$
$$W_{tot} = 200u$$



Process parameters needed to be corrected. (TBAR, EPSILON) Therefore, the DC curves are not longer fitting with this version of the model

Conclusion

- Physics-based models are necessary for mmW applications and plays a crucial role in industrial deployment.
- ASM-HEMT was tested on 2 different GaN technologies from 2 different foundries, and it proved to be a good candidate for RF-GaN (single geometry). There are many publications available showing a good fitting for a single geometry (but not for a set of geometries!)
- The DC scaling rules have been effectively integrated at the Verilog-A level of the ASM-HEMT CMC model.
- Initial validation of width scaling has been successfully conducted using DC measurements.
- Some weaknesses were identified in the CV/RF characteristics in on-state.
  - Reason: a few process parameters were set incorrectly at the beginning of this work due to lack of information about the technology.

Next steps

- It is necessary to restart from scratch, following the steps below:
  - Setting the correct process parameters from the beginning.
  - The reference geometry for the initial ASM model parameter extraction should be one of the biggest geometries (narrow channel effects)
  - The scaling parameters should be extracted while looking simultaneously at the DC and CV/RF characteristics.

- Other axes for improvement:
  - Self-heating effect (the DC characterization was done up to Vd=3V and Vg=0)
  - Trapping effect
  - Large signal measurement/simulations
  - Noise

Thank you.

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